SHARP TECHNICAL MANUAL

TY0T9VC-A30GB

VHS VIDEO CASSETTE RECORDER

(PAL SYSTEM)

SERIES	MODEL NO.	VIDEO HEAD
VC-A10 Series	VC-A10E, G(BR), S(BR), Q(BR), X, Y(BR), VC-A11N	2-head system
VC-A30 Series	VC-A30G(BR), S(BR), GM(BR), SM(BR), QM(BR), SV(BR), HM, LM, X, W, NZ, BI, BZ, BP, YM(BR), B, VC-A31N, VC-A32D, VC-A35X, NZ	
VC-A40 Series	VC-A40G(BR), S(BR), GM(BR), SM(BR), HM, QM(BR), YM(BR), W, K, VC-A45X, W, NZ, VC-A255GM	
VC-A50 Series	VC-A50GM(BR), SM(BR), YM(BR)	4-head system
VC-A60 Series	VC-A60G(BR), S(BR), WT, X, NZ, SM(BR), GM(BR), HM, YM(BR), VC-A61NT, VC-A62DT	

CONTENTS

1. SYSTEM CONTROLLER LSI (2-HEAD SYSTEM) 2
2. SYSTEM CONTROLLER LSI (4-HEAD SYSTEM) 21
3. TIMING CHART 49
4. TIMER CIRCUIT (RH-IX0581GEZZ) 55
5. TIMER CIRCUIT (RH-IX0589GEZZ) 64
6. BLOCK DIAGRAM 77

SHARP CORPORATION

1. SYSTEM CONTROLLER LSI

- 2-head system: RH-iX0801GEZZ, RH-iX0802GEZZ

1. TERMINAL ASSIGNMENT

I/O	Terminal Name	Name	No.
	+5V	Vcc	64
PWM O	DRUM PHASE ERROR (D-APC)	PWM0	63
PWM O	DRUM SPEED ERROR (D-AFC)	PWM1	62
PWM O	CAPSTAN PH ERR (C-APC)	PWM2	61
PWM O	CAPSTAN SPD ERR (C-AFC)	PWM3	60
C-MOS	DRUM APC MUTE (L)	P54	59
C-MOS	CAPSTAN APC MUTE (L)	P55	58
C-MOS	SEARCH (L)	P56	57
C-MOS	CTL GAIN SW	P57	56
I	PG (V.HSW/A.HSW) M.M	PG-ADJ	55
I	CAPSTAN FG	C-FG	54
I	DRUM FG	D-FG	53
I	DRUM PG	D-PG	52
I	VERTICAL SYNC (L)	Vsync	51
O	VIDEO H.SW.P	V.HSW	50
TERNARY O	FV	FV	49
I	PB-CTL	PB-CTL	48
O	REC CTL ⊖	R-CTL	47
O	REC CTL ⊕	R-CTL	46
TERNARY O	CTL THRESHOLD CHANGE	P10	45
I	SHORT IN	P11	44
C-MOS	PAL/SECAM(H)	P12	43
C-MOS	MESECAM(H)	P13	42
C-MOS	AHC(H)	P14	41
C-MOS	HiFi CTL(L)	P15	40
C-MOS	BAIS CTL(H)	P16	39
C-MOS	GND CTL	P17	38
N-CH	V-Tuner(L)	P00	37
N-CH	A-Tuner(H)	P01	36
N-CH	ALPB(L)	P02	35
N-CH	EE(L)	P03	34
N-CH	PCON(L)	P04	33

RH-iX0801GEZZ or RH-iX0802GEZZ

No.	Name	Terminal name	I/O
1	P47	SYNC DET (H)	I
2	P46	START SENSOR	I
3	P45	END SENSOR	I
4	P44	DEW SENSOR	I
5	P43	OPERATION KEY	A/D I
6	AD2	CASSETTE SW	A/D I
7	AD1	CAM SW	A/D I
8	AD0	FUNCTION SELECT	A/D I
9	P37	REEL SENSOR	I
10	A.HSW	AUDIO H.SW.P	O
11	SO	SYSCON SERIAL DATA	O
12	SCLK	TIMER SERIAL CLK	I
13	SI	TIMER SERIAL DATA	I
14	P32	SYSCON READY (L)	O
15	P31	COUNTER PULSE	C-MOS
16	INTO	SP(H)	C-MOS
17	P27	AUDIO MUTE (H)	C-MOS
18	P26	LOADING FWD CTL	C-MOS
19	P25	LOADING REV CTL	C-MOS
20	P24	BRAKE SOLENOID	C-MOS
21	P23	DRUM MUTE (L)	TERNARY O
22	P22	CAPSTAN CTL	TERNARY O
23	P21	CAPSTAN REV	O
24	P20	CURRENT LIMITER	TERNARY O
25	TEST	+5V	
26	RESET	SYSCON RESET (L)	I
27	X1	CLK INPUT	I
28	X2	CLK OUTPUT	O
29	P07	CAPSTAN PU (L)	N-CH
30	P06	CAPSTAN UL (L)	N-CH
31	P05	VTR(L)	N-CH
32	GND	G N D	

2. TERMINAL DESCRIPTION

port	Control signal	Specification	
1	SYNC DET (H)	◎ This signal is output from the external Sync Det circuit to notify whether Hsync of input video signal is present or not to determine weak electric field. (1) With Hsync, weak electric field (L) is "H". Without Hsync, weak electric field (L) is "L".	
2	START SENSOR	◎ This signal detects the start of tape. (1) If the leading edge of START SENSOR is detected (i) The stop processing is executed if operation is in the REW status. (ii) The short rewind is stopped if operation is in the REC, PAUSE and SHORT REW status. (2) In the STOP mode, the tape is wound up at rapid feed until the START SENSOR goes "L". However, if the START SENSOR does not go "L" in 5 seconds after of rapid feed, the stop processing is executed. (3) The START SENSOR is used to recognize the cassette down. See the END SENSOR item.	
3	END SENSOR	◎ This signal detects the end of tape. (1) If the leading edge of END SENSOR is detected (i) The tape is automatically rewound in the ON mode. (ii) The tape is wound up and ejected in the TIMER REC mode. (2) In the STOP mode, the tape is rewound until the END SENSOR goes "L". However, if it does not go "L", the stop processing is executed. (3) The cassette down is recognized with the END SENSOR and START SENSOR signals. The controller recognizes the eassette down when (CASSECON DOWN) • ((END SENSOR)+(START SENSOR))="H".	
4	DEW SENSOR	◎ This signal indicates the condense status. (1) The controller recognizes the condense status when the DEW SENSOR is "H", and inhibits mechanical operation. However, the following keys are active even in the condense status. •POWER •EJECT/LOAD •TV/VTR (2) When the DEW SENSOR goes "H", the mechanism moves to the EJECT position, and the following transition occurs. When PCON (L) = "L", DRUM MUTE (L) goes "H". When PCON (L) = "L", DRUM MUTE (L) goes "L". (3) When the DEW SENSOR goes "L", the mechanism moves to the STOP position.	

port	Control signal	Specification
5	ORERATION KEY	
6	CASSETTE SW	◎These terminals contain a comparator and D/A converter to provide the A/D conversion function with 8 resolu-tions (ports 5 and 8) and 6 resolutions (ports 6 and 7) in order to convert analog signals into digital ones.
7	CAM SW	
8	FUNCTION SELECT	• The following lists switches that correspond to the A-H keys in the D/A conversion circuit shown later.

SW/SPEC.	Mainframe key	VS spec.	SLOW function	x2 speed
A	REC	Fixed	Fixed	Provided
B	PAUSE	Fixed	Variable	Provided
C	FF	Variable	Fixed	Provided
D	PB	Variable	Fixed	None
E	REW	Fixed	Fixed	None
F	STOP	Variable	Fixed	None
G	EJECT	Fixed	Variable	None
H	POWER	Variable	Variable	None, *
SW"OPEN"	SW OFF	Fixed	Fixed	None

* Note 1: The x2 speed function is provided for RH-IX0801GEZZ, but not for RH-IX0575GE.

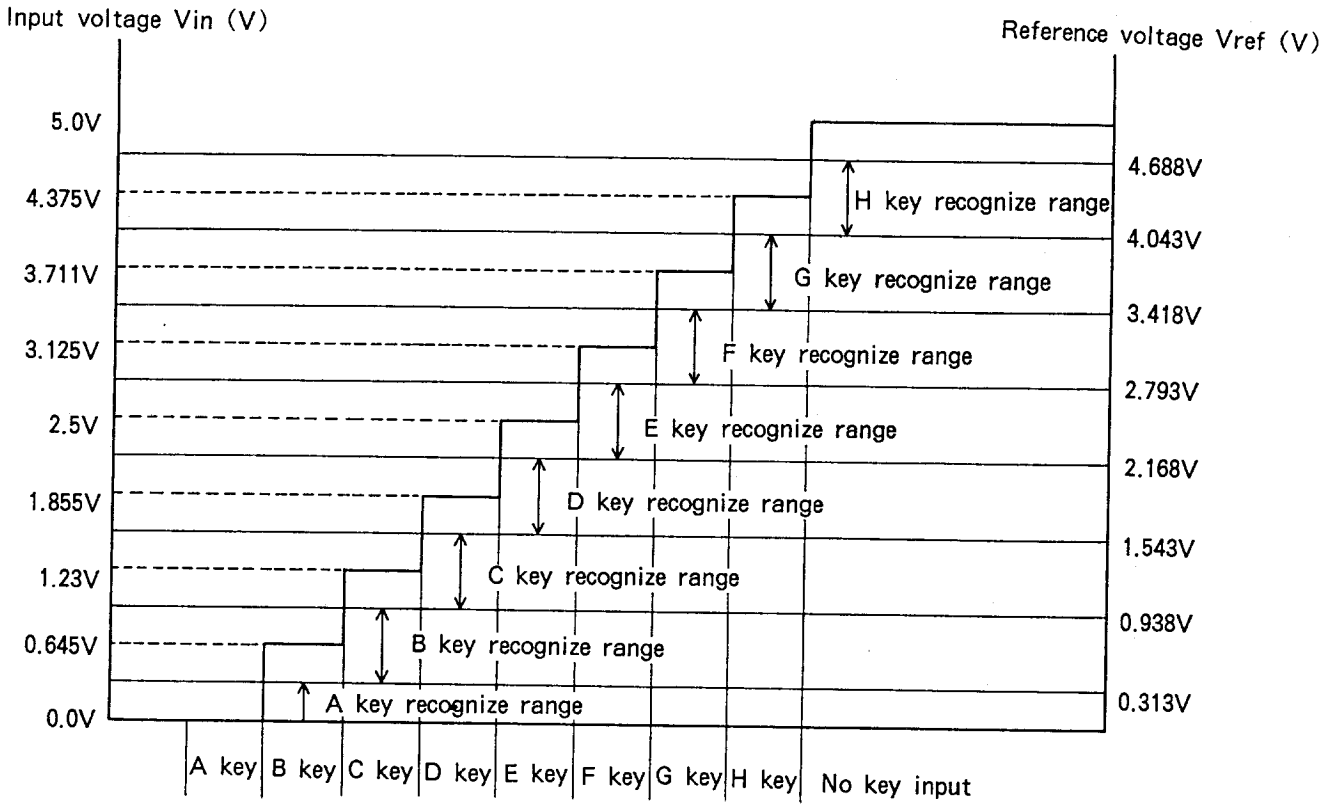
•Switches associated with A-H keys in the D/A conversion circuit.

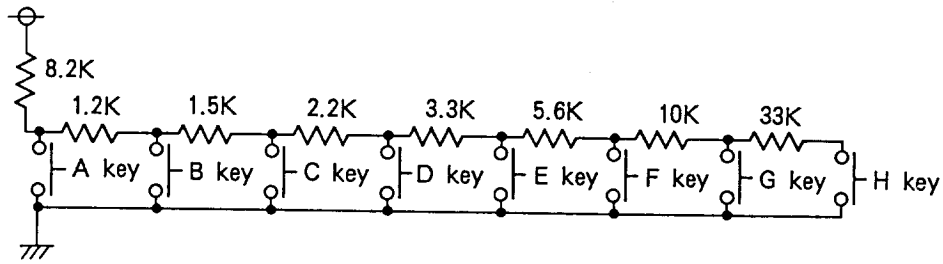
Input terminal / SW	MECHAPOSI. SW INPUT
A	CA SW
B	HF SW
C	FF SW
D	LD SW
E	PB SW
F	PU SW
SW "OPEN"	SW OFF

<CASSECON SW> (See the cassette control circuit)

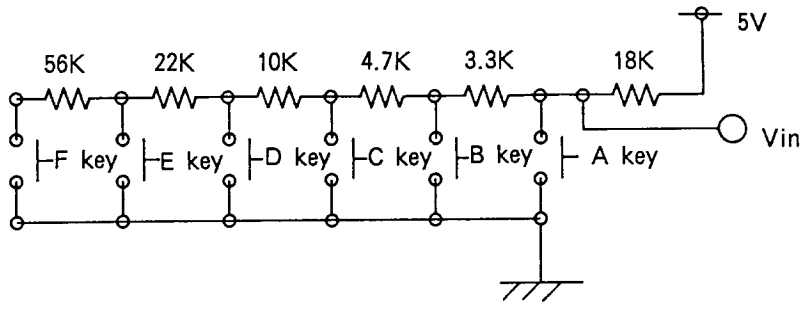
Type / SW	CASSECON /AUTO CASSECON	Specification
A	CASSECON SW (Detects loading start)	ON : Cassette loading start OFF: Other than above
B	AUTO LOAD SW (Detects cassette loading status)	ON : Cassette is loaded OFF: Non auto load, CASSECON or cassette is not loaded
C	REC. TIP SW (Detects erasure prevention tip condition)	ON : Tip is broken. OFF: Tip is present.
D	(Detects CAS. unit mounting status)	•With the unit mounted, DSW is always ON. •Without the unit, all switches are OFF.

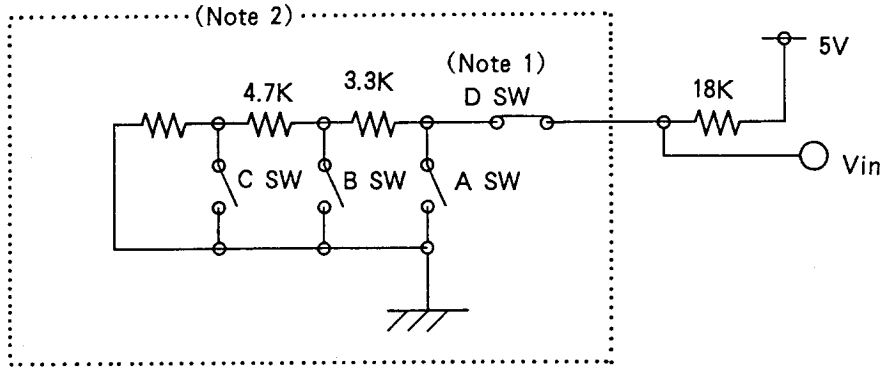
D/A Conversion Circuit and Threshold Voltage
(MAINFRAME KEY/FUNCTION SELECT KEY INPUT)



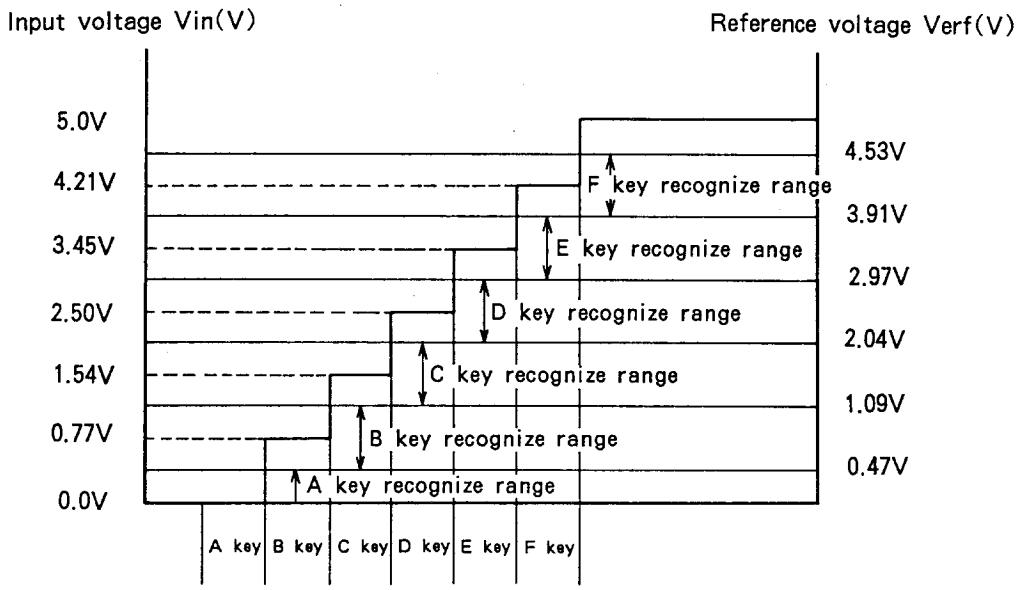


D/A Conversion Circuit (MECHAPOSI. SW/ CASSECON SW)





<Cassette Control Circuit>

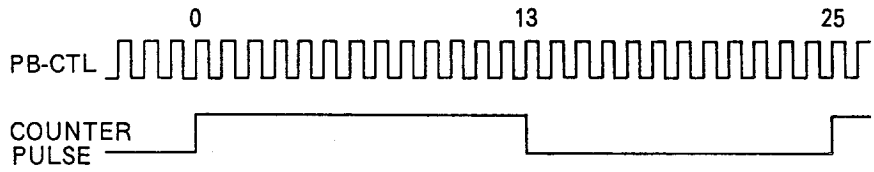
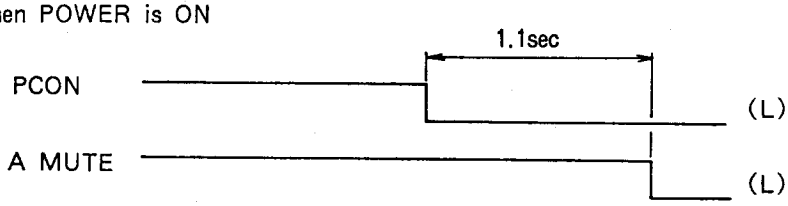
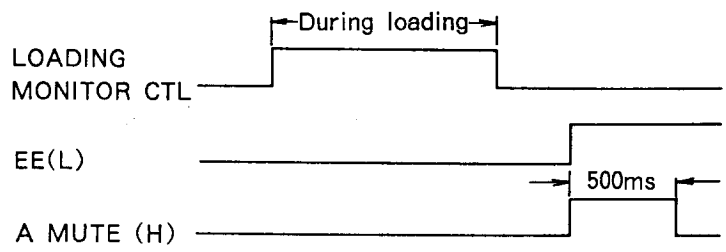


(Voltage setting value A-1)

Input voltage "Vin" and reference voltage "Vref" for each switch

<table>
<tr><th>port</th><th>Control signal</th><th>Specification</th><th></th></tr>
<tr><td></td><td></td><td>[CAM SW]
◎For the loading mechanism position and its mode, see 5-24.

[CASSETTE SW]
◎This detects the cassette loading and timing and the REC.tip condition.
[CASSECON SW]
(1) The A SW detects cassette loading start with the slider in UP status.
(2) The B SW is always OFF.
(3) The D SW is conceptual switch and it is always ON when CAS. unit is mounted.
[REC. TIP SW]
(1) The SW is ON when the tip is broken, and it is OFF when the tip is present.
(2) When the tip is broken, the cassette is ejected if you try to activate the "REC/TIMER REC" mode.
(See Tip broken cassette auto eject function)</td><td></td></tr>
<tr><td>9</td><td>REEL SENSOR</td><td>◎This signal detects the reel head status when the reel head is to be run.
(1) The reel head is to be run under either of the following conditions.
(i) When loading is completed
•PB
•REC
•VSF
•VSR
•x2 speed
(ii) When unloading is completed
•FF
•REW
(2) Under either of the above conditions, if the REEL SENSOR INPUT does not transit within the time specified for each mode, the stop processing is executed.
<table><tr><th>Mode</th><th>Shut-off time</th></tr><tr><td>PB(SP) REC(SP)
FF REW x2 x1.5</td><td>5.0sec</td></tr><tr><td>PB(LP) REC(LP)</td><td>10.0sec</td></tr><tr><td>VSR VSF</td><td>1.2sec</td></tr></table>(3) The loose tape detect processing counts the edges of reel pulses to be input using the REEL SENSOR.</td><td></td></tr>
<tr><td>10</td><td>AUDIO HSW</td><td>◎This terminal outputs H.SW pulses for HiFi.</td><td></td></tr>
</table>

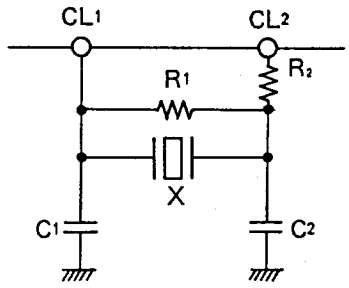
port	Control signal	Specification	
11 12 13 14	SYSCON SERIAL DATA SERIAL CLOCK TIMER SERIAL DATA TIMER READY (L)	◎These signals control the serial data transfer between timer IC and SYSCON IC. (1) The TIMER READY (L) goes "L" every 23.4 msec to transfer 8 bits x 5 bytes. (2) For the serial data transfer, the SYSCON SERIAL DATA is set at the trailing edge of serial clock from the timer IC after the TIMER READY (L) goes "L", and the TIMER SERIAL DATA is input at leading edge of serial clock. The TIMER READY (L) goes "H" after 8-bit data input has completed. (3) The "H" status of TIMER READY (L) must last for more than 1.3 msec.	
15	COUNTER PULSE	◎This terminal outputs the PB-CTL divided into 25. The timer IC counts the real time using this divided pulses. The PB-CTL signal is input from port 48, and its divided pulses are as shown below. 	
16	SP(H)	◎This signal goes "H" in the SP mode, and it goes "L" in the LP mode.	
17	A MUTE (H)	◎This signal stops audio output. (1) The A MUTE (H) is always "H" when PCON (L) = "H". (2) When POWER is ON  (3) After PB LOADING has completed  (4) In the PB mode, when a trick playback key is turned on, the A MUTE (H) goes "H" immediately to enable the trick playback.	

<table>
<tr><th>port</th><th>Control signal</th><th>Specification</th><th></th></tr>
<tr><td></td><td></td><td>(5) When a trick playback (STILL, SLOW, VSF, VSR, x2 SPEED) is reset, the A MUTE (H) goes "L" about 1000 ms after the loading mechanism moves to the position for PB mode.
(6) When PB mode is cancelled with EE (L) in "H" status, the A MUTE (H) is "H" for 500 msec.</td><td></td></tr>
<tr><td>18

19</td><td>LOADING MOTOR FWD CTL
LOADING MOTOR REV CTL</td><td>(1) These signals control the rotational direction of loading motor.

The following table shows a combination of control signal and mode.
<table>
<tr><th>CNT signal / Mode</th><th>LOADING MOTOR FWD CTL</th><th>LOADING MOTOR REV CTL</th></tr>
<tr><td>Loading motor stop</td><td>L</td><td>L</td></tr>
<tr><td>Loading motor forward</td><td>H</td><td>L</td></tr>
<tr><td>Loading motor reverse</td><td>H</td><td>H</td></tr>
</table>
(2) When mechanical operation is in stop status
•LOADING MOTOR FWD CTL = "L"
•LOADING MOTOR REV CTL = "L"
(3) To protect loading motor from overcurrent, the following function is provided.
•2.5-sec shutoff in the CASSECON operation mode
•7-sec shutoff in the loading arm operation mode
(4) The shutoff function causes the LOADING MOTOR FWD CTL and LOADING MOTOR REV CTL to go "L", and keeps the loading motor stopped at that position until an operation key is pressed. However, the loading motor reverses immediately to eject the cassette if the CASSECON is running forward.
(5) CASSECON operation
(i) When a cassette is loaded, it is ejected immediately unless the CASSECON moves to the CASSECON down position within 2.5 sec, or the shutoff function operates unless the CASSECON moves to the CASSECON up position within 2.5 sec.
(ii) When a cassette is ejected, it is loaded immediately unless the CASSECON moves to the CASSECON up position within 2.5 sec, or the shutoff function operates unless the CASSECON moves to the CASSECON down position within 2.5 sec.</td><td></td></tr>
</table>

port	Control signal	Specification	
20	BRAKE SOLENOID	◎This signal turns on or off the solenoid for brake. (1) When the BRAKE SOLENOID is "H", the brake solenoid is attracted. (2) At the FF • REW position when REW key is pressed, REW is displayed and the LOADING MOTOR FWD goes "L" while the LOADING MOTOR REV goes "H". Then, the BRAKE SOLENOID goes "H" after the mechanism moves to the brake release position. (3) At the FF•REW position when FF key is pressed, FF is displayed and the brake release processing is executed in the same manner as (2) above. (4) When a cassette is already loaded and also the END SENSOR or START SENSOR is "H", the brake release processing is executed in the same manner as (2) above. (5) When a loose tape is detected, the brake release processing is executed in the same manner as (2). (6) At the PB•REC position, with EE (L) in "H" status, when REW key is pressed, VSR is displayed, the BRAKE SOLENOID goes "H" and the mechanism moves to the VSR position. After that, the BRAKE SOLENOID goes "L". Then, when the VSR mode is reset, the tape running is stopped and BRAKE SOLENOID goes "H", and it goes "L" after the mechanism moves to the PB•REC position. (7) The BRAKE SOLENOID goes "L" just before the CAPSTAN UL (L) goes "H" in (2), (3) and (4) in the item CAPSTAN UL (L). (8) The BRAKE SOLENOID goes "L" just before FF/REW is reset.	
21	DRUM MUTE (L)	◎This signal controls the drum motor, and the drum motor stops when DRUM MUTE (L) is "L". (1) At the FF/REW position, when PB, VSR, VSF, STILL, SLOW, x2, or REC is displayed, the DRUM MUTE (L) goes "Z", and loading starts after 500 msec. (2) At the PB•REC position, when STOP, FF or REW is displayed, unloading starts. After unloading has completed, the DRUM MUTE (L) goes "L". (3) For the rolling acceleration in the SLOW/STILL mode, see very slow feed timing chart.	
22	CAPSTAN CTL	◎This signal controls (accelerate/stop) the capstan motor. (1) STILL/SLOW mode (i) STILL mode: CAPSTAN CTL = "H" (ii) SLOW/VSF mode : See very slow feed timing chart (2) Other than SLOW/STILL (i) Capstan motor run : CAPSTAN CTL = "Z" (ii) Capstan motor stop: CAPSTAN CTL = "L"	

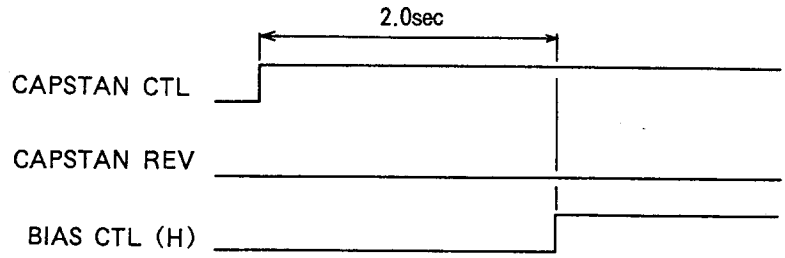
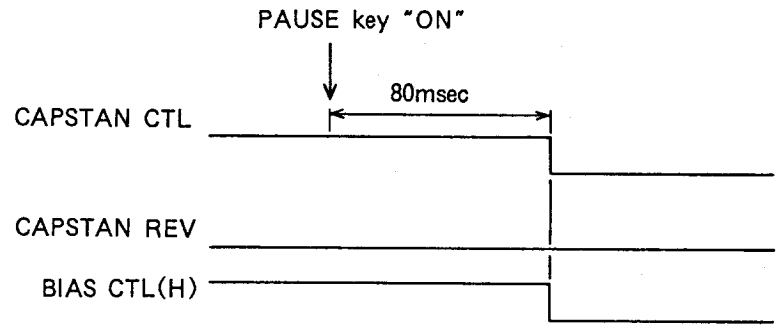
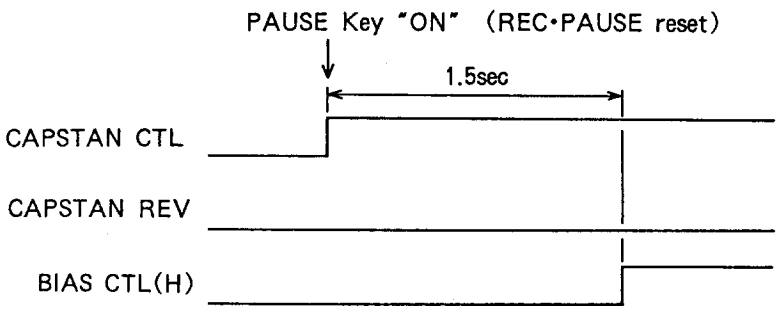
<table>
<tr><th>port</th><th>Control signal</th><th>Specification</th><th></th></tr>
<tr><td>23</td><td>CAPSTAN REV</td><td>◎This signal determines rotational direction of capstan motor.
<table>
<tr><th>Control signal / Mode</th><th>CAPSTAN CTL</th><th>CAPSTAN MOTOR REV</th></tr>
<tr><td>Capstan motor stop</td><td>L</td><td>L</td></tr>
<tr><td>Capstan motor FWD</td><td>Z</td><td>L</td></tr>
<tr><td>Capstan motor REV</td><td>Z</td><td>H</td></tr>
</table></td><td></td></tr>
<tr><td>24</td><td>CURRENT LIMIT</td><td>◎This signal limits the torque (current) of capstan motor.
(1) When PCON (L) = "H"
(i) STILL mode : CURRENT LIMIT = "Z"
(ii) SLOW/VSF mode : See very slow feed timing chart
(iii) Other than above modes : CURRENT LIMIT = "H"</td><td></td></tr>
<tr><td>25</td><td>TEST</td><td>◎Test pin for IC.
Usually, this pin is connected to Vcc.</td><td></td></tr>
<tr><td>26</td><td>RESET</td><td>◎Reset pin for IC.
• RESET = "L": IC is in reset status.
• RESET = "H": IC operates.</td><td></td></tr>
<tr><td>27
28</td><td>CLOCK IN
CLOCK OUT</td><td>The built-in system clock generating circuit outputs clock signal (4.433619MHz) When connected to the crystal as shown below.
 

X : 4.433619MHz
(RCRSB0116GEZZ) · · · · VC-A10 Series
or RCRSB0002CEZZ
C1 : 22PF
C2 : 22PF
R1 : 1MΩ
R2 : 470Ω</td><td></td></tr>
<tr><td>29</td><td>CAPSTAN PU (L)</td><td>◎ This signal controls the rotation torque of reel.
(1) The CAPSTAN PU (L) that controls the voltage for the capstan motor torque is output in the following timing.
(i) When the mechanism moves from PB•REC to VSR position
(ii) When the mechanism moves from VSR to PB•REC position
(iii) At idling movement (oscillating motion)
(iv) From tape winding up immediately after cassette loading to idling movement
(v) Idling movement at REC → REC•PAUSE</td><td></td></tr>
</table>

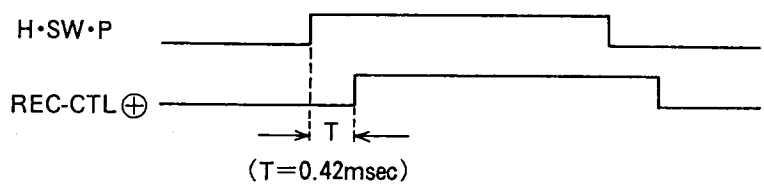
port	Control signal	Specification	
30	CAPSTAN UL (L)	◎ This signal controls the rotation torque of reel (1) The CAPSTAN UL (L) controls the torque control voltage applied to the capstan motor. It goes "L" during unloading, or when FF or FEW is started or a tape is wound up in the EJECT mode. (i) At the PB•REC position, when STOP/FF/REW mode is activated, the loading motor is reversed. After 500 msec, the CAPSTAN UL (L) goes "L". Then, at the brake release position, the CAPSTAN UL (L) goes "H" and the capstan motor stops. (ii) At the FF•REW position, when FF key is pressed, FF is displayed and the brake is released. Then, the CAPSTAN UL (L) goes "L" to rotate the capstan motor froward. After 500 msec, the CAPSTAN UL (L) goes "H". (iii) At the FF•REW position, when REW key is pressed, REW is displayed and the brake is released. Then, the CAPSTAN UL (L) goes "L" to reverse the capstan motor. After 500 msec, the CAPSTAN UL (L) goes "H". (2) In the loose tape detection or leader tape winding processing, the CAPSTAN UL (L) is "L" for 500 msec when the tape is running. However, if the above processing ends within 400 msec, the CAPSTAN UL (L) goes "H" immediately. (3) Idling movement at the start of loading (4) Loose tape winding up processing (300 msec) just after cassette loading (5) Loose tape winding up processing during EJECT operation (6) Loose tape prevention at the time of PB → STOP	
31	VTR MODE (L)	◎ This signal changes over signals connected to the RF converter. (1) When VTR MODE (L) = "L", the playback signal from video tuner or video tape is connected. (2) When VTR MODE (L) = "H", the signal from antenna (VHF) is connected. (3) When PCON (L) = "H", the VTR MODE (L) goes "H". (4) When PCON (L) = "L" and the TV/VTR select key is pressed, • VTR MODE (L) goes "L" if it is in "H" status. • VTR MODE (L) goes "H" if it is in "L" status. (5) In the PB mode, when STOP key is pressed, (i) VTR MODE (L) is kept "L" if it is in "L" status when a playback image is output. (ii) VTR MODE (L) is kept "H" if it is in "H" status when a playback image is output.	
32	Vss	◎Vss pin (GND). Connect to GND.	

<table>
<tr><th>port</th><th>Control signal</th><th>Specification</th><th></th></tr>
<tr><td>33</td><td>PCON (L)</td><td>◎This signal controls power supply (for drive system).
(1) With POWER in OFF status, when the POWER key is pressed, the PCON (L) goes "L". However, the POWER key is inactive in the timer standby mode.
(2) With the POWER in ON status, when the POWER key is pressed, the PCON (L) goes "H". However, the PCON (L) is kept "L" during operation of mechanism, and it goes "H" at the following position.
• STOP position
• Slider up position
(3) In the timer standby mode, when the timer start data of timer serial data is detected, the PCON (L) goes "L" and REC is displayed. (Timer recording start)
(4) In the timer standby mode, the PCON (L) is "H".
(5) If PCON (L) is in "H" status when the loading motor, cassette motor or capstan motor is driven, it goes "L". Then, it goes "H" after end of motor drive.</td><td></td></tr>
<tr><td>34</td><td>EE (L)</td><td>◎ This signal changes over screen between EE and playback
(1) The EE signal changes over the audio/video outputs between EE and PB. The EE (L) in "L" status selects signals supplied from tuner (EE screen) or the EE (L) in "H" status selects signals supplied from video head (PB screen).
(2) At the PB•REC position, when EE (L) is "L" in the PB group mode, the capstan motor runs forward, then after 1 sec, the EE (L) goes "H".
(3) When the PB group mode is reset, the EE (L) goes "L".</td><td></td></tr>
<tr><td>35</td><td>ALPB (L)</td><td>◎ This signal changes over mode between REC and PB.
(1) At the PB•REC position, the ALPB (L) is "L" in the PB group mode (PB, STILL, SLOW, VSF/R, x2).
(2) When the PB group mode is reset, the ALPB (L) goes "H".</td><td></td></tr>
<tr><td>36
37</td><td>A-TUNER (H)
V-TUNER (L)</td><td>◎ These signals change over mode between TUNER/SIMUL/AUX
Its control follows the serial data from timer IC.

Mode change between TUNER/SIMUL/AUX
<table>
<tr><th>Mode / Bit</th><th>TUNER mode</th><th>SIMUL mode</th><th>AUX mode</th><th>Don't care</th></tr>
<tr><td>V-TUNER bit (T_{27})</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>A-TUNER bit (T_{43})</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
</table>
Pin 36 follows A-TUNER (T_{43}). When T_{43} = "1", A-TUNER(H) = "H".
Pin 37 follows V-TUNER (T_{27}). When T_{27} = "1". V-TUNER(H) = "H".</td><td></td></tr>
<tr><td>38</td><td>GND CTL</td><td>◎ This signal sets the bias of PB-CTL line to GND in the PB mode.
The GND CTL goes "L" when BIAS CTL (H) = "H" in the REC mode.
It goes "H" in the mode other than above.</td><td></td></tr>
</table>

port	Control signal	Specification	
39	BIAS CTL (H)	◎ This signal controls start/stop of audio/video signal recording. (1) The timing for the REC is shown in (1), (2), (3), and (4) below. (2) When the PB key is pressed in the REC mode, the mode is changed to PB mode 100 msec after the processing shown in (2) below has completed.	
40	HiFiCTL (L)	◎ This signal controls start/stop of HiFi recording. (1) After end of loading, the REC mode is started in the following timing.  (2) The REC reset and the REC•PAUSE timing are as shown below.  (3) The REC•PAUSE mode is reset in the following timing.  (4) The REC mode is reset in the same timing as (2).	

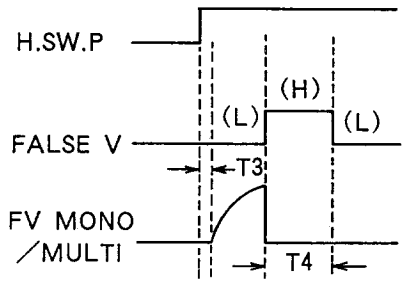
<table>
<tr><th>port</th><th>Control signal</th><th>Specification</th></tr>
<tr><td>41</td><td>A•H•C (H)</td><td>◎ The signal controls external circuit to prevent the drum head from clogging.
It is output under the following condition.
(1) When initial loading of cassette is executed
(2) When the EJECT key is pressed in the loading status (PB, REC mode).
(3) When initial loading is executed by reset.</td></tr>
<tr><td>42
43</td><td>PAL/SECAM(H)
MESECAM(H)</td><td>◎ These signals control the color circuit according to the serial data transferred from the timer IC.

(1) Broadcast system mode selection
<table>
<tr><th>Broadcast system / Bit</th><th>PAL</th><th>SECAM</th><th>ME-SECAM</th><th>AUTO</th><th>Not used</th></tr>
<tr><td>PAL(T_{45})</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>MESECAM(T_{46})</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
</table>
Pin 43 follows the PAL (T_{45}). When T_{45} = "1", the PAL/SECAM (H) is "H".
Pin 42 follows the MESECAM (T_{46}). When T_{46} = "1", the MESECAM (H) is "H".
(2) After reset, the AUTO mode is active and the PAL/SECAM (H) is "L" and MESECAM (H) is "L" until start of serial data transfer with the timer IC.</td></tr>
<tr><td>44</td><td>SHORT IN
INPUT</td><td>◎ This signal detects shortcircuit in the PCON power line. The signal in "H" status is always input.</td></tr>
<tr><td>43</td><td>CTL
THRESHOLD
CHANGE</td><td>◎ This terminal outputs ternary signals indicating PB-CTL threshold according to the mode.
<table>
<tr><th>Output</th><th>Mode</th></tr>
<tr><td>High</td><td>VS-F/R FF/REW</td></tr>
<tr><td>"Z" high impedance</td><td>PB x 2</td></tr>
<tr><td>Low</td><td>SLOW/STILL</td></tr>
</table></td></tr>
<tr><td>46
47</td><td>REC-CTL ⊕
REC-CTL ⊖</td><td>◎ These signals control PB-CTL writing in the REC mode.
(1) Both REC-CTL ⊕ and REC-CTL ⊖ are in "Z" (high impedance) status in all modes except when the BIAS CTL (H) is "H" in the REC mode.
(2) The REC-CTL ⊕ is inverted output of REC-CTL. ⊖
(3) The PB-CTL writing timing is as shown below.
 

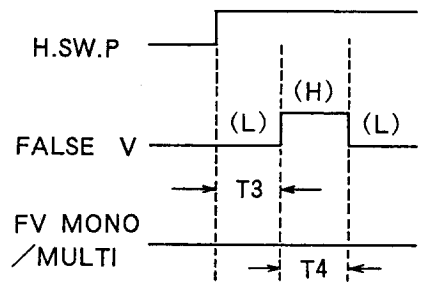
(T=0.42msec)</td></tr>
</table>

port	Control signal	Specification
48	PB-CTL	◎ PB-CTL input terminal. (1) This signal is used as a trigger that applies reverse torque of very slow feed. (2) It along with CAPSTAN FG evaluates the recording speed. (3) If the leading edge of PB-CTL is not detected for 120 msec in the PB mode, the blue mute request is sent to the timer IC. (4) It is used for the capstan phase servo.
49	FALSE VERTICAL SYNC	◎ In the trick mode (VS-F/R), FV/FH is generated for synchronization. (1) The FV is generated in the VS-F/R mode, during mechanism movement when mode is changed from PB to VS-R or when VS-R is reset, during mode hold period for VS-F/R reset, or in the SLOW/STILL or x2 mode. (2) The generation is as shown below. (Note: For the H.SW.P, both leading and trailing edges are used.)

C mode (Variable FV binary output)



D mode (Fixed FV binary output)



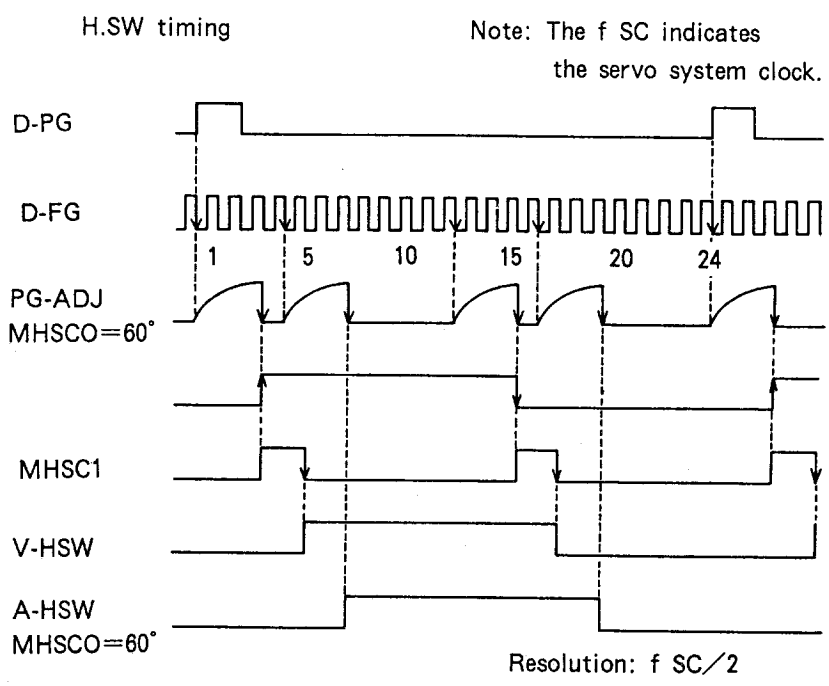
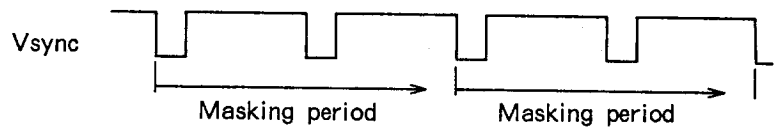
Note: Z: high impedance

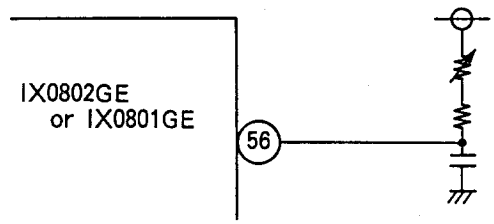
(3) Relation between mode and output pulses

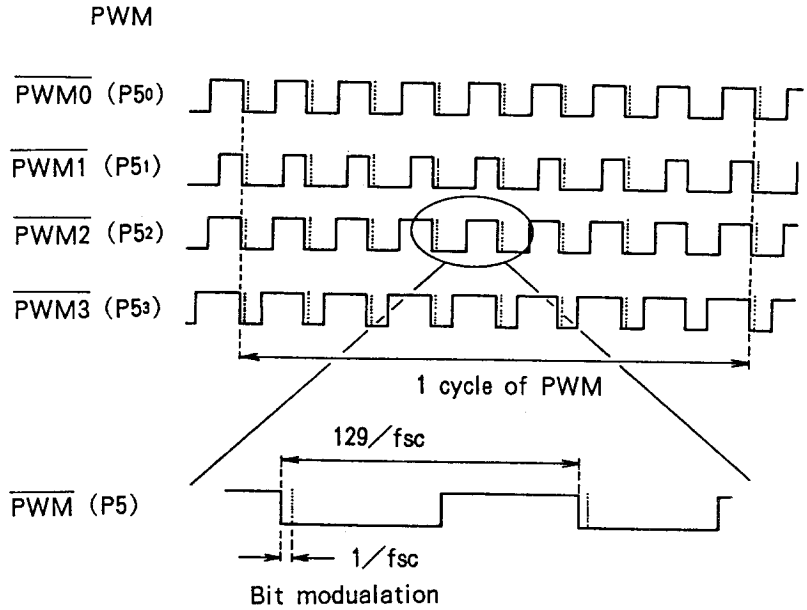
Mode	REC mode	H.SW.P	
		Leading edge	Trailing edge
VS-F/R	SP	D mode	D mode
	LP	D mode	D mode
STILL/SLOW	SP	D mode	C mode
	LP	D mode	C mode
x2	SP	D mode	C mode
	LP	D mode	C mode

(3) False V pulse width in each mode (Unit: μs)

Mode	H.SW.P	SP mode			LP mode		
		T_3	T_4	T_5	T_3	T_4	T_5
SLOW/STILL (Middle speed period)	Leading	270	316		270	316	
	Trailing		316	141		316	170
SLOW/STILL (Other than above period)	Leading	270	316		270	316	
	Trailing		316	141		316	170
x2	Leading	270	316		270	316	
	Trailing		316	141		316	170
VS-F/R	Leading	216	316		216	316	
	Trailing	216	316		216	316	

port	Control signal	Specification	
50	VIDEO H.SW.P	◎ This signal selects CH1 or CH2 by the head amplifier. (1) The H.SW.P is generated in the 1-PG/FG division system. (2) The H.SW.P is generated in the following timing. 	
51	V SYNC	◎ This is a reference signal to control the drum phase in the REC mode. (1) The V SYNC is input in the 2-division system. (2) To prevent noise, the V SYNC input is masked for duration of 90% of frame frequency after 2-divided V SYNC is entered. 	
52	DRUM PG	◎ This signal ajusts phase between H.SW.P and video head (CH1) attached to the drum. (1) The PG adjustment starts by the trailing edge of drum FG after the leading edge of drum PG is detected. With this operation, the output phase of H.SW.P is adjusted. * For the timing, see the Port 50, H.SW.P.	
53	DRUM FG	◎ This signal controls the drum speed. (1) It is input to generate the H.SW.P. The H.SW.P "H" and "L" are output alternately for every 12 FG. * For the timing, see the Port 50, H.SW.P. (2) It is a reference signal to control the drum speed, and it controls the time from leading edge to trailing edge using the system clock. The speed error is controlled by the Port 62, DRUM SPEED ERROR (PWM).	

port	Control signal	Specification	
54	CAPSTAN FG	Capstan FG signal input terminal. (1) This signal evaluates the recording speed for playback signal. (2) It is a reference signal to control the capstan speed. It, according to the speed ratio, divides the CAPSTAN FG multiplied by 2 internally, then it controls the time from its leading edge and next leading edge by the f SC/4 clock. The speed error is controlled by the Port 60, CAPSTAN SPEED ERROR (PWM).	
55	PG MONO. MULTI	◎ This signal adjusts installation error of video head against the drum PG, and controls the H.SW.P output timing.  (1) The PG MONO/MULTI input is started at the leading edge of DRUM FG after detecting the leading edge of DRUM PG.	
56	CTL GAIN SW	◎ This signal changes over the PB-CTL amplifier gain in the FF/REW mode. (1) In FF/REW mode : CTL GAIN SW = "H" In other than above mode : CTL GAIN SW = "L"	
57	SEARCH (L)	◎ This signal changes over the gain for PB-CTL signal. (1) In the VS-F/R mode, the SEARCH (L) = "L".	
58	CAPSTAN APC MUTE (L)	◎ This signal fixes the capstan phase system to 2.5V during mode transition. (1) It fixes the capstan phase system to 2.5V when either of the following modes is reset. • VSF rush and reset • FF • VSR rush and reset • REW • STOP • STILL/SLOW • Loading • Unloading (2) The CAPSTAN APC MUTE period at the time of VSF/VSR rush and reset is about 500 msec.	
59	DRUM APC MUTE (L)	◎ This signal fixes the drum phase system control to 2.5V. (1) It fixes the drum phase system to 2.5V during the following operation. • VSF rush and reset • FF • VSR rush and reset • REW • STOP • Unloading (2) The DRUM APC MUTE period at the time of VSF/VSR rush and reset is about 500 msec.	

port	Control signal	Specification	
60	CAPSTAN SPEED ERROR	◎ The signal indicating the capstan speed servo error is output in the PWM method. (1) At 10-bit quantized fsc=4.433619MHz, it is output at high speed PWM of 34.6kHz. (2) The capstan speed servo error is output. The error which is the CAPSTAN FG multiplied by 2 is output as PWM.  Resolution: f SC	
61	CAPSTAN PHASE ERROR	◎ The signal indicating the capstan phase servo error is output in the PWM method. (1) At 10-bit quantized fsc=4.433619MHz, it is output at high speed PWM of 34.6kHz. (2) The capstan phase servo error is output. • In the PB mode, the time gap between leading edge of V-H.SW.P and PB-CTL to be input is set to the target value • In the REC mode (including FF and FEW), the time gap between CAPSTAN APC counter that counts with fsc/16 and CAPSTAN PG that is the divided CAPSTAN FG is set to the target value.	
62	DRUM SPEED ERROR	◎ The signal indicating the drum speed servo error is output in the PWM method. (1) At 10-bit quantized fsc=4.433619MHz, it is output at high speed PWM of 34.6kHz. (2) The drum speed servo error is output. • The rising time of DRUM FG is set to the target value.	

port	Control signal	Specification	
63	DRUM PHASE ERROR	◎ The signal indicating the drum phase servo error is output in the PWM method. (1) At 10-bit quantized fsc=4.433619MHz, it is output at high speed PWM of 34.6kHz. (2) The drum phase servo error is output. • In the REC mode, the time gap between DRUM APC counter synchronizing with V SYNC and rising time of V-H.SW.P is set to the target value. • In the PB mode, the time gap between internal reference frequency and rising time of V-H.SW.P is set to the target value.	
64	Vcc	◎ Vcc Terminal	

2. SYSTEM CONTROLLER LSI

- 4-head system: RH-iX0579GEZZ

2-1. System Controller Terminal Allocation.

I/O	Terminal Name	Name	No.
O(C-MOS)	GND CTL	P20	64
O(3S)	FV	P21	63
O(C-MOS)	FV CTL	P22	62
O(C-MOS)	X2	P23	61
O(C-MOS)	CTL GAIN SW (L)	P24	60
O(3S)	DRUM CTL	P25	59
O(3S)	CURRENT LMT	P26	58
O(3S)	CAPSTAN CTL	P27	57
O(N-CH)	CAPSTAN RVS (H)	P00	56
O(N-CH)	CAPSTAN PU (L)	P01	55
O(N-CH)	CAPSTAN UL (L)	P02	54
O(N-CH)	LOADING FWD CTL	P03	53
O(N-CH)	LOADING RVS CTL	P04	52
O(N-CH)	BRAKE SOLENOID	P05	51
O(N-CH)	SERVO S DATA	P06	50
O(N-CH)	SERVO S CLOCK	P07	49
O(N-CH)	TRANSIT (H)	P10	48
O(N-CH)	H. AMP SW	P11	47
O(N-CH)	CHROMA ROTARY	P12	46
O(N-CH)	AHC (L)	P13	45
O(N-CH)	PB AUDIO (H)	P14	44
O(N-CH)	HiFi CTL	P15	43
O(N-CH)	AUDIO MUTE (L)	P16	42
O(N-CH)	EE (L)	P17	41
I	$\overline{\text{SYNC DET (H)}}$	P50	40
I	REEL SENSOR	P51	39
I	START SENSOR	P52	38
I	END SENSOR	P53	37
I	INDEX IN	P54	36
I	DEW SENSOR	P55	35
I	NC	P56	34
I	PB CTL	P57	33

RH-iX0579GEZZ

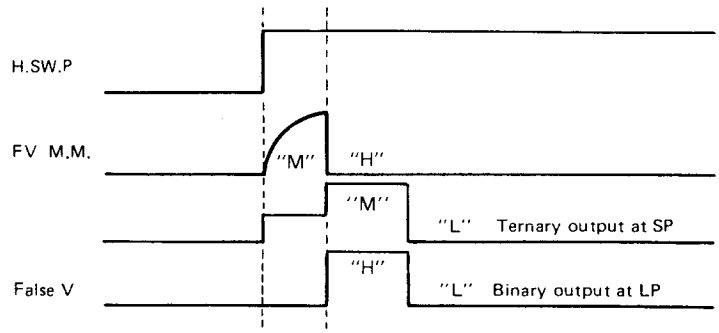
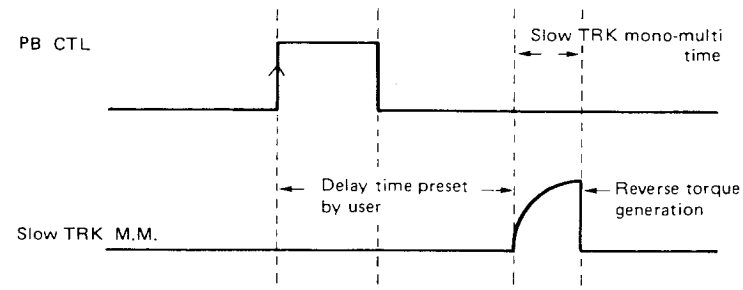
No.	Name	Terminal Name	I/O
1	Vcc	5V	
2	AVss	GND	
3	Vref	A/D REF, VOLTAGE	
4	D-A	COUNTER F/R	O(C-MOS)
5	PWM	BEEPER	O(N-CH)
6	P63	AL PB (L)	O(N-CH)
7	P62	BIAS CTL (H)	O(N-CH)
8	P61	POWER CTL (L)	O(N-CH)
9	P60	VCR (L)	O(N-CH)
10	AN7	CAM SW	I (A/D)
11	AN6	CASSETTE SW	I (A/D)
12	AN5	AUTO FUNCTION	I (A/D)
13	AN4	NC	I (A/D)
14	AN3	FV M.M.	I (A/D)
15	AN2	SLOW/STILL TRK	I (A/D)
16	P41	SPEED DET	I
17	P40	COUNTER RESET	O(N-CH)
18	SRDY	S.T READY (L)	O(N-CH)
19	CLK	T.S CLOCK	I
20	SOUT	S.T DATA	O(N-CH)
21	SIN	T.S DATA	I
22	CNTR	SEARCH (L)	O(N-CH)
23	INT2	ENVELOPE DET (L)	I
24	P31	ENVELOPE DET	I
25	P30	H.SW.P	I
26	INT1	H.SW.P (L)	I
27	CNVss	GND	
28	ACL	ACL (L)	I
29	XIN	CLOCK IN	I
30	XOUT	CLOCK OUT	O
31	Ø	NC	O
32	Vss	GND	

Figure 2-1. Bottom View

2-2. TERMINAL DESCRIPTION

Pin No.	Control Signal	Specifications
1	5V	Vdd terminal
2	GND	AVss terminal (GND) To be connected to GND
3	A/D REF VOLTAGE	Reference voltage for A/D converting
4	COUNTER F/R	It is a control signal offering the tape running direction to the timer IC. (1) Counter CTL = "H" : Reverse turn Counter CTL = "L" : Positive turn (2) Other than the model below should be identical to the capstan motor direction. Namely, in case of capstan reverse turn- "H", counter CTL = "H" is applied. • Cue sound countermeasures for FF/REW-Stop, etc. (Idler neck swing) • Idler neck swing • Inversion brake time for VS release (3) In the mode below, the following are to be taken to adjust to the tape running direction. (For use of real time counter) • At loading ..... Counter CTL = "L" • Eject position/Stop position ..... Counter CTL = "L"
5	BEEPER	This output shows the time of confirmation sound output when the operating key is pressed. • Confirmation sound "ON time" = "H" • Confirmation sound "OFF time" = "L" **[System controller]** (1) The time of outputting a confirmation sound is 47 msec. (2) The timing of outputting a confirmation sound is to be at receiving of keys below. • Power key • TV/VCR key • Eject key • Stop key • FF key • PB key • REC key • Pause key • REW key • Slow key • Double speed key • At INDEX writing (optional writing) **[Timer]** (However, the confirmation sound output is only when the timer serial data takes buzzer request.) (1) The time of outputting a confirmation sound is 47 msec. and 1 sec. (2) To output the 47 msec. confirmation sound, it is done when 47 msec. short sound buzzer 1 is present with the timer serial data. (Refer to the timer ref. material for the operating key outputting a short sound buzzer request.) • For the time of confirmation sound, it is shorter than the above value at Slow/Still.
6	AL PB (L)	A signal to select REC mode with PB mode (1) In case of PB-system mode (PB, Still, Slow, VS-F/R, double speed) at PB. REC position, AL PB (L) = "L" is applied. (2) When the PB-system mode is released, it should be AL PB (L) = "H".

Pin No.	Control Signal	Specifications
7	BIAS CTL (H)	A signal to control start/end of recording of video/audio signal
8	POWER CTL (L)	A signal to control the power (supply) (controlling a driving-system power) (1) When the Power key is pressed at Power "OFF", it should be PCON (L)="L". However, in case of timer stand-by, the Power key should be in-effective. (2) When the Power key is pressed in ON mode, it should be PCON (L)="H". However, during mecha-operation, PCON (L)="L" is continued, and PCON (L)="H" is applied at the next mecha-position. • Stop position • Slider Up position (3) At timer stand-by, if the timer start data of timer serial data is detected, it should be PCON (L)="L", making REC display. (Timer recording start) (4) At timer stand-by, it should be PCON (L)="H". However, in VPS Interrupt mode, PCON (L)="L" is applied. (5) For driving of loading motor, cassette motor or capstan motor, if PCON (L)="H" is present, it should be made PCON (L)="L", and after driving, it is made PCON (L)="H". (6) In case of EE (L)="L" and PCON (L)="L", if weak electric field (L) input="L" continues for 30 min., it is automatically to be PCON (L)="H", allowing the mis-power-OFF preventive function to be effected.
9	VCR (L)	Control signal to switch on and off the signal to come to the RF converter. (1) Signal from the video tuner or playback signal from the video tape fed in with VCR (L) signal at "L". (2) Antenna input (VHF) signal fed through in with VCR (L) signal at "H". (3) VCR (L) signal at "H" with power control (L) signal at "H". (4) With power control (L) signal at "L", the TV/VCR selector key switches VCR (L) signal: • From "H" to "L". • From "L" to "H". (5) When the Stop key is pressed during playback mode, the following are obtained. i) If the VTR mode (L)="L" at output of playback screen, VTR mode (L)="L" is continued. ii) If the VTR mode (L)="H" at output of playback screen, VTR mode (L)="H" is continued.
10	CAM SW	
11	CASSETTE SW/REC TIP	This terminal has the A/D converting function of 6-resolution for analog voltage by the comparator (IC built-in) and D/A converter. (5 to 8)
12	AUTO FUNCTION	
13	NC	To be connected to Vdd or GND
14	FV M.M	It is intended to adjust the delay amount from the edge of H.SW.P to the generation of false vertical synchronous signal.

Pin No.	Control Signal	Specifications
		(1) Normally, "L" is outputted. (2) After detection of H.SW.P edge, the terminal is made to be "Z" (High impedance) and the mono-multi input taken. When recognized as "H", the mono-multi input is stopped and the terminal to be "L".  **Figure 2-2.**
15	SLOW/STILL TRK	It is intended to adjust the reverse torque generating timing at Slow/Frame advance. The preset is inputted to this terminal. (1) Normally, "L" is outputted. (2) At frame advance, when it detects the rising edge of PBCTL signal, it allows the delay time preset by user to pass by. Then, the terminal is selected to "Z" (High impedance) and such a mono-multi input started. When recognized as "H", the mono-multi input is stopped and the terminal to be "L".  **Figure 2-3.**
16	SPEED DET	Switches shown corresponding to A-F keys of D/A converting circuit

Key \ Input terminal	Mecha-posi. SW input	Speed detection input	Function selection input
A	CA SW	SP mode	Variable speed VS/Auto OFF
B	HF SW		Variable speed VS/Auto Repeat
C	FF SW	LP mode	Fixed Vs/Auto OFF
D	LD SW		Fixed VS/Auto Repeat
E	PB SW		Not used
F	PU SW		Not used
ALL SW "OFF"	SW OFF mode		Not used

Auto Power OFF: Auto power OFF function
Auto Repeat: Auto repeat playback function

Table 2-1.

Pin No.	Control Signal	Specifications

[Cassette controller SW]

Refer to cassette controller circuit. (Fig. 2-4.)

Type / SW	Cassette controller/Auto cassette controller	Specifications
A	Cassette controller SW (Insertion start detection)	ON: Cassette insertion start OFF: Other than above
B	Auto load SW (Cassette fit-in state detection)	ON: Cassette fit-in state OFF: Non-auto load cassette controller or cassette not fitted in
C	REC. Tip SW (Mis-erasing preventive tab detection)	ON: Preventive tab broken OFF: Preventive tab present
D	(CAS. Unit fit-in state detection)	• D-SW to be always "ON" at unit fit-in state • All SWs to be "OFF" without unit

Table 2-2.

D/A Converting circuit (Main body SW/CAM. SW/Function selecting SW/Cassette controller SW)

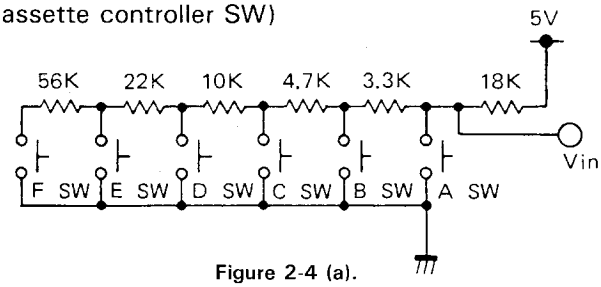
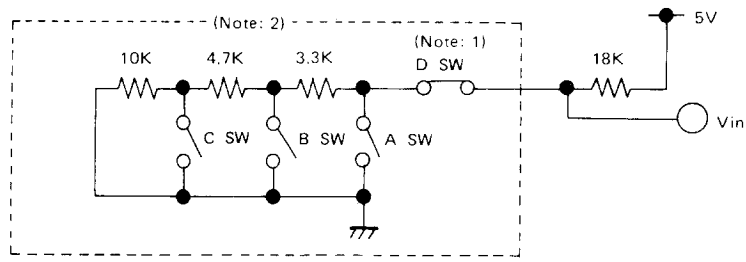


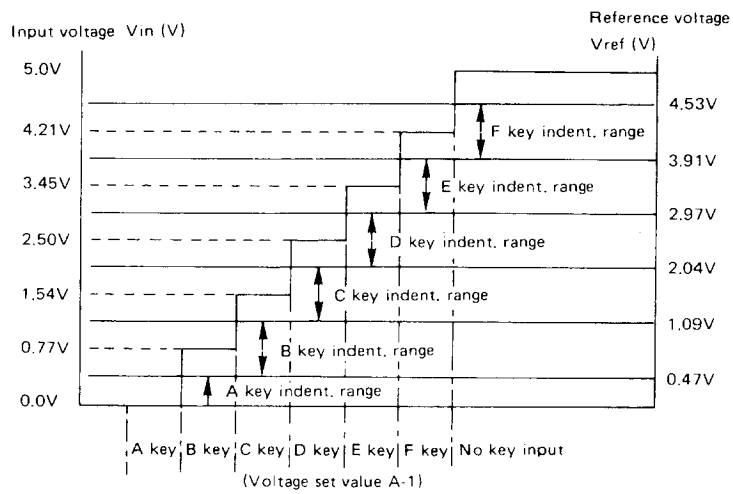
Figure 2-4 (a).



Cassette control circuit

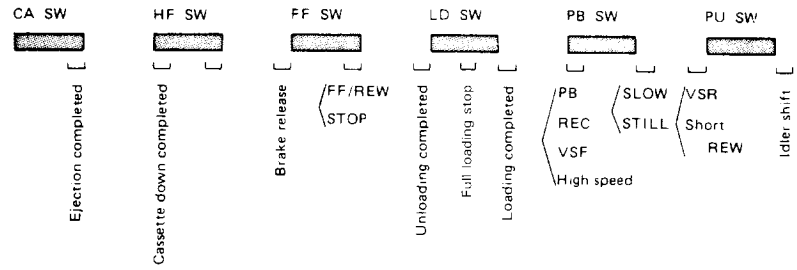
Note 1: The D switch is kept on all the time.
Note 2: The block framed with broken line is the cassette controller unit.

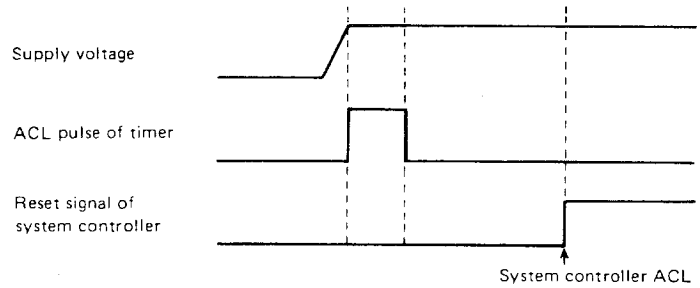
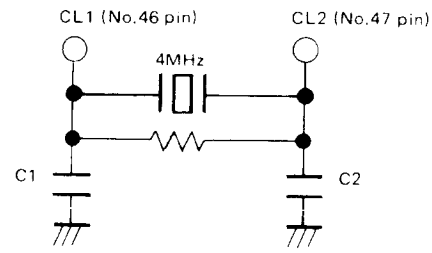
Figure 2-4 (b).



Input voltage (Vin) VS. reference voltage (Vref) with each switch.

Figure 2-4 (c).

Pin No.	Control Signal	Specifications
		 Figure 2-4 (d). **(CAM SW input)** • Refer to Fig. 2-4 for L-mecha. mecha-posi. and mode. **(Cassette control SW/REC Tip input)** • Timing of cassette insertion/Detection of REC. Tip state **(Cassette controller SW)** (1) SW A detects start of cassette insertion in slider UP condition. (2) SW B is intended for Auto load cassette controller and "ON" when the cassette is fitted in slider UP condition. For normal-type cassette controller, it is always "OFF". (3) SW D is conceptual and always "ON" when the CAS. unit is fitted in. **(REC Tip SW)** (1) It is "ON" at REC Tip broken and "OFF" at REC Tip present. (2) It takes Eject immediately, if the "REC/timer REC" mode is to be started at REC Tip broken. (Tab-broken cassette/Auto-Eject function) **(Speed detection input)** Input to detect a tape speed data of 4H/2H (1) Refer to the preceding para. of "A/D terminal description" for the relation between the recording mode and the voltage level to be inputted. (2) The data inputted is transferred to the timer IC as below. i) In Stop/REC mode, the data of speed detection input is made ineffective, and the data of recording mode selected by timer is made to be a serial signal, transferred and displayed. ii) At replay by PAL 2HEAD, the following codes are trasferred to the servo IC, instructed by "Audio 8CH spec. treatment" from the timer. • SP mode (Speed identification permitted) at Audio 8CH spec. treatment • SP fixed (Speed identification prohibited) at Audio 8CH spec. no-treatment
17	COUNTER RESET (H)	Control signal to reset the CTL frequency dividing IC. (ONLY VC-A60G, S, H, Y, VC-A50G, S, Y)
18	S.T READY (L)	Refer to Page 39.
19	T.S CLOCK	It is a control signal intended for serial transfer between the timer IC and the system controller IC. (1) It should be timer READY (L)="L" every 23.4 msec., and 8 bit x 5 byte transferring is taken. (2) For serial transfer, after timer READY (L)="L" has been made, the system controller serial data is set by trailing edge of serial clock from timer IC, and the timer serial data is inputted by rising edge of serial clock. And then, after input of 8 bit data, it should be timer READY (L)="H". (3) The time of timer READY (L)="H" is 1.3 msec. min. (4) For serial data, refer to page 38.
20	S.T DATA	
21	T.S DATA	

Pin No.	Control Signal	Specifications
22	SEARCH (L)	It is a control signal for selecting the gain of PB CTL signal. (1) In Video-Search F/R mode, it should be Search (L)="L".
23	ENVELOPE DET (L)	Reference signal for head amplifier/chroma rotary switching output. To be given out of the head amplifier module. (1) Used to control the head amplifier/chroma rotary switching output with the envelope comparison signal input as reference in each mode.
24	ENVELOPE DET	
25	H.SW.P.	Sensor input intended to detect the state of the drum to be rotated. (1) Head switching pulse to detect if the drum is running. (2) Drum remains running with drum speed-up at "Z" (high impedance) from loading start to unloading end. (3) If head switching pulse input stays in the state (2) above for 1.6 seconds, the head is stopped. It is the reference signal of FV output in trick mode (VSF/R, x 2, STILL/SLOW). (1) In trick mode, FV output is taken at the rising and trailing edges of HSW.P input (HSW.P). (2) A signal allowing start of frame advance.
26	H.SW.P.(L)	
27	GND	CNVss terminal (GND) To be connected to GND
28	ACL (L)	It is an initial resetting terminal of microcomputer, and allows the microcomputer to be initial-reset by applying the low voltage. In addition, with system controller reset signal, initial resetting is possible by connecting such a signal to the ACL terminal by the timer microcomputer. The timing of system controller reset signal on timer microcomputer is shown Fig. 2-5.  **Figure 2-5.**
29 30	CLOCK IN CLOCK OUT	The system clock generating circuit of microcomputer is built in, and the clock signal (4 MHz) is obtained by connecting the ceramic resonator shown Fig. 2-6.  **Figure 2-6.**
31	NC	NC terminal: Terminal should to be open.

Pin No.	Control Signal	Specifications
32	GND	Vss terminal (GND) To be connected to GND
33	PB CTL	Reference signal taking playback blue mute (1) Unless PB CTL rising edge can be detected during 120 msec. in PB mode, a blue mute request is taken to the timer IC. (2) Ref. signal for determining a time (61 ± 2 pulses) of "INDEX signal writing" (3) Detection signal for identifying a recorded tape (tab broken cassette) in Full Auto function • A signal causing reverse torque generation at frame advance
34	NC	To be connected to Vdd or GND.
35	DEW SENSOR	An input terminal to detect any dew situation (1) When the dew sensor is equal to "H", it identifies as dew situation and prohibits any mecha. actuation. However, the following keys should be effective regardless of dew situation. • Power • Eject/Insertion • TV/VTR (2) When the dew sensor is equal to "H", the mecha. position is moved to Eject position and done as follows: PCON (L)="L" ..... Drum mute (L)="H" PCON (L)="H" ..... Drum mute (L)="L" (3) When the dew sensor is equal to "L", the mecha. position is moved to Stop position.
36	INDEX IN	This input is to detect cue signal in INDEX mode. (1) "H" is inputted on cue recording section. (H to be 20 msec. min.) (2) By timer operation, Intro search (Interval search) and Index search are set. i) Setting of Intro search (Interval search) When the FF/REW key is pressed, it is shifted to Intro search. When the cue signal input "H" is detected during FF/REW mode, it comes to be PB mode during 7 sec. and is re-shifted to the FF/REW mode, continuing the cue signal input. ii) Release of Intro search (Interval search) When the mode is cleared by the timer, Intro search is released at once, continuing the current mode. When the mode key (STOP/FF/REW/PB/REC/SLOW/double speed key) is pressed during Intro search, the Intro search mode is released, allowing mode shifting. iii) Index search When the number of skips is set by Index search, the INDEX signal is detected, and then it is transmitted to the timer IC by the system controller SIO.
37	END SENSOR	A signal to detect a tape end (1) For detection of rising edge of end sensor input: i) In case of ON mode with cassette IN, auto-rewinding is taken. ii) During timer REC, Eject is taken after leader tape winding. (2) If in Stop mode, the tape is rewound and the leader tape wound until the end sensor input is "L". However, unless the end sensor input is "L" even after continuous rewinding for 5 sec., stop processing is taken.

<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td></td><td></td><td>(3) Cassette-down is judged by the end sensor input and the next start sensor input as follows:
(Cassette controller down). ((<u>End sensor</u>) + (<u>Start sensor</u>))="H"
In such a case, cassette-down is recognized.</td></tr>
<tr><td>38</td><td>START SENSOR</td><td>A signal to detect a tape start
(1) For detection of rising edge of start sensor input:
i) In case of REW mode, stop processing is taken.
ii) If during REC/PAUSE short rewinding, short rewinding is interrupted.
(2) If is Stop mode, the tape is rapidly advanced and the leader tape wound until the start sensor input is "L". However, unless the start sensor input is "L" regardless of continous rapid-advance for 5 sec., stop processing is taken.
(3) The start sensor input is utilized for cassette-down recognition. Refer to the paragraph of end sensor input.</td></tr>
<tr><td>39</td><td>REEL SENSOR</td><td>It is a sensor input intended to detect the reel stand situation when it is to be turned.
(1) The situation subject to a reel stand turn is as follows:
i) For loading completion:
• PB
• REC
• VSF
• VSR
• Double-speed
ii) For unloading completion:
• FF
• REW
(2) In such conditions, unless the reel sensor input changes within the time of each mode shown below, stop processing is taken.
<table>
<tr><th>Mode</th><th>Shut-Off Time</th></tr>
<tr><td>SP-PB/SP-REC/FF/REW/Double-speed/1.5-time speed</td><td>5.0 sec.</td></tr>
<tr><td>LP-PB/LP-REC</td><td>10.0 sec.</td></tr>
<tr><td>Video Search Rewind/Video Search Reverse</td><td>1.2 sec.</td></tr>
</table>
Table 2-3.
(3) For processing of tape slack detection, the edge of reel pulse to be inputted utilizing the reel sensor is to be counted.</td></tr>
<tr><td>40</td><td><u>SYNC DET</u> (H)</td><td>It is an identifying terminal for weak electric field, being a signal to be outputted from the external Sync Det circuit for Hsync existence of input video signal.
(1) For Hsync presence, it is weak electric field (L)="L".
For Hsync not present, it is weak electric field (L)="H".
(2) Input of weak electric field (L) is effective in case of EE (L)="H".
(3) In case of EE (L)="L" (EE screen), if the weak electric field (L)="H" continues for 120 ms., it is to be a blue screen applied. (The timer IC takes OSD for application. However, that is only when the blue back ON/OFF SW is "ON".)
(4) In Stop condition with PCON (L)="L", if the weak electric field (L)="H" continues for about 30 min., PCON (L)="H" is applied. (However, unless any execution instruction (T36) from timer IC is done, it is ineffective. At selection of Full Auto, T36="1".)</td></tr>
</table>

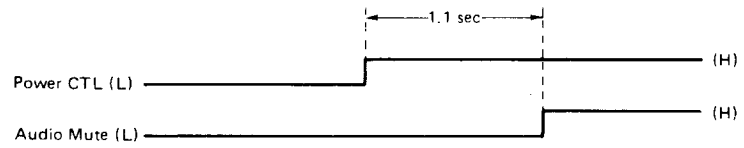
<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td>41</td><td>EE (L)</td><td>A signal of selecting between EE screen and playback screen
(1) The EE signal is intended to select the signal, i.e. the video/audio output is to be EE or PB, and thus in case of EE (L)="L" it selects to the signal (EE screen) to be transmitted from the tuner, and also at EE (L)="L" it selects to the signal (PB screen) to be transmitted from the video head.
(2) At PB. REC position, if it is PB-system mode and EE (L)="L", EE (L)="H" is applied about 1 sec. after positive turn of capstan motor.
(3) If the PB-system mode is released, it should be EE (L)="L".</td></tr>
<tr><td>42</td><td>AUDIO MUTE (L)</td><td>A signal to stop any audio output
(1) At Power CTL (L)="H", it should be Audio mute (L)="L" at any time.
(2) For Power "ON":
 

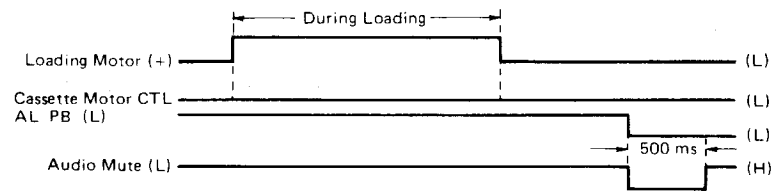
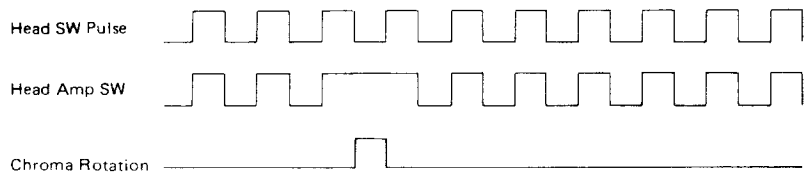
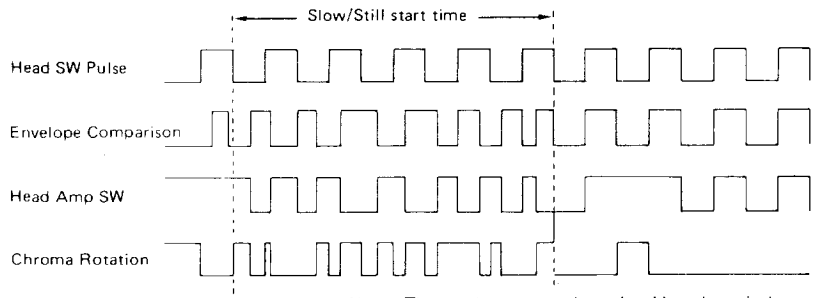
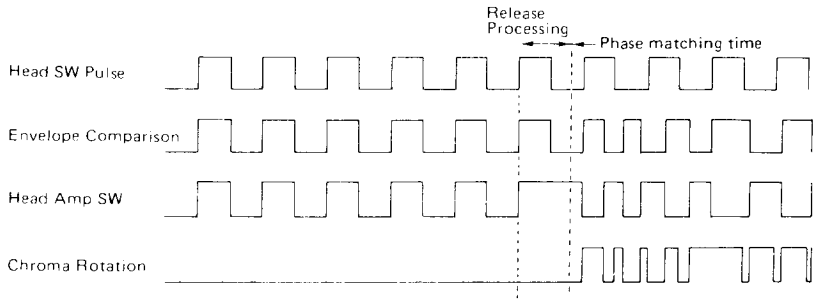
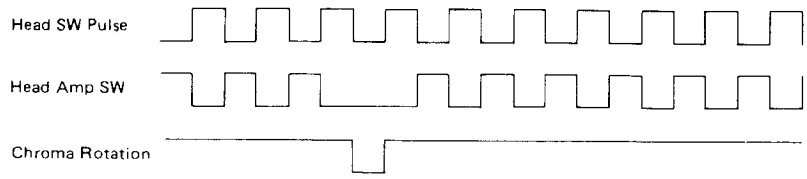
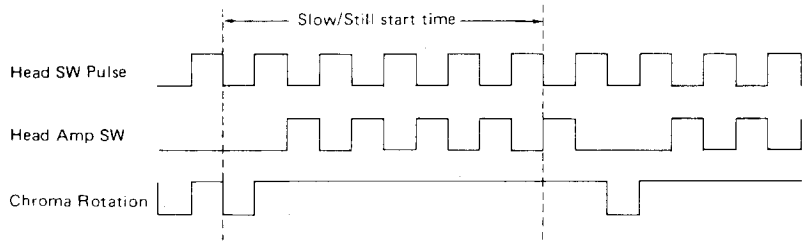
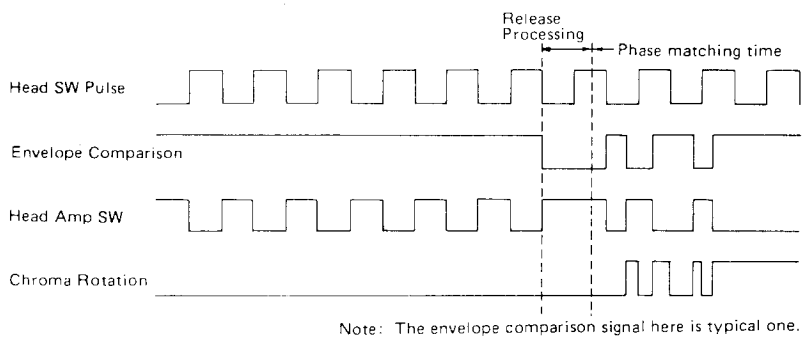
Figure 2-7.
(3) After PB loading end:
 

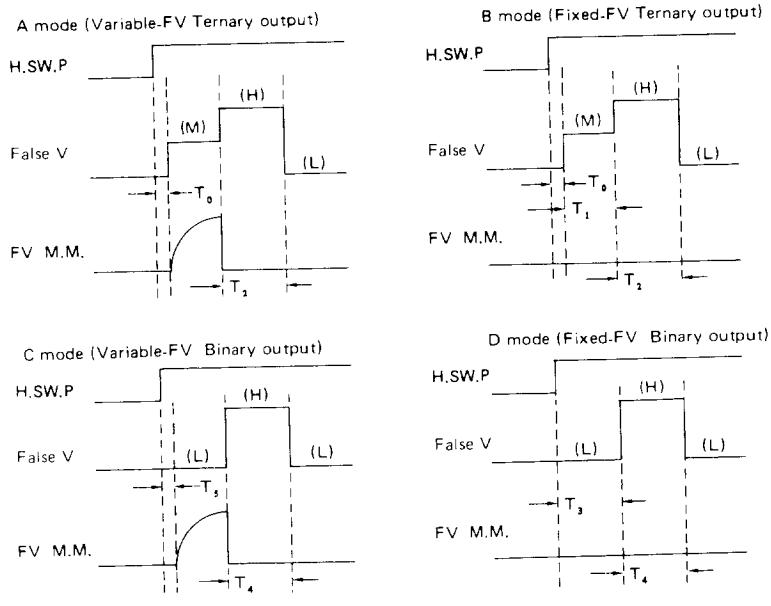
Figure 2-8.
(4) In PB mode, when the trick playback (Still, Slow, VSF, VSR & double speed) key is turned "ON", A mute (L)="L" is applied immediately, shifting to trick playback.
(5) When trick playback is released, it is moved to the mecha-posi. of PB mode, and then after about 1,000 ms, A mute (L)="H" is applied.
(6) When the PB mode is released with EE (L)="H" condition, A mute (L) should be ="L" for 500 msec.</td></tr>
<tr><td>43</td><td>HiFi CTL</td><td>Not used.</td></tr>
<tr><td>44</td><td>PB AUDIO (H)</td><td>Audio muting at PB Audio (H) → "H"
At EE (L) → "L"
<table><tr><th>Pin ⑩ $\overline{\text{SYNC DET (H)}}$</th><th>PB AUDIO (H)</th></tr><tr><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td></tr></table>Table 2-4.
At EE (L) → "H"
<table><tr><th>Pin ⑫ FV CTL</th><th>PB AUDIO (H)</th></tr><tr><td>H</td><td>H</td></tr><tr><td>L</td><td>L</td></tr></table>Table 2-5.</td></tr>
</table>

Pin No.	Control Signal	Specifications
45	AHC (L)	The signal controls external circuit to prevent. The drum from clogging. It is output under the following condition. (1) When initial loading of cassette is executed. (2) When the EJECT key is pressed in the loading status. (PB, REC and Full loading stop mode.) (3) When initial loading is executed by reset.
46	CHROMA ROTARY	Terminal to select chroma. (1) Right channel: "H" (6° azimuth head side). (2) EXOR logic for head switching pulse and head amplifier switching signal.
47	H.AMP SW	Output to select between SP and LP heads. (1) SP mode: "H" LP mode: "L" (2) Head amplifier switching control signal at "L" in LP mode. (3) Inverted envelope comparison input signal (pin ㉔) to be outputted at VS-F/R in SP mode. (4) Signal to be outputted according to record mode of each step during slow/frame advance. **(SP mode)** • This signal remains in phase with head switching pulse during frame advance.  **Figure 2-9.** • This signal remains in anti-phase with envelope comparison signal at the start of slow/still mode.  Note: The envelope comparison signal here is typical one. **Figure 2-10.** • The envelope comparison signal is inverted after the slow/still mode is cleared.  Note: The envelope comparison signal here is typical one. **Figure 2-11.**

Pin No.	Control Signal	Specifications
		(LP mode) • This signal remains in anti-phase with head switching pulse during frame advance.  **Figure 2-12.** • The following timing is set up at the start of slow/still mode.  **Figure 2-13.** • The envelope comparison signal is inverted after the slow/still mode is cleared.  Note: The envelope comparison signal here is typical one. **Figure 2-14.**
48	TRANSIT (H)	When transferring from VS FWD and VS RVS modes to PB mode, it continues to be "H" for approx. 1,400 ms. Used to cope with colour dislocation
49	SERVO S. CLOCK	(1) The following are the method of data transfer to servo IC. The servo IC outputs the data of 21 bits to latch the servo/display serial data at rising edge of servo/display serial clock. Then, the serial output is completed by making servo/display serial data="H" at the final clock trailing edge. (2) For mode and data, refer to page 37.
50	SERVO S. DATA	
51	BRAKE SOLENOID	It is a signal for controlling the brake solenoid ON/OFF. (1) This signal is intended to control the brake solenoid ON/OFF, and in case of brake solenoid="H", the brake solenoid is made to be attracted. (2) When the REW key is pressed at FF.REW position, REW display is made, and it makes loading motor positive-turn CTL="L" and loading motor reverseturn="H", and after movement to brake release posi., brake solenoid="H" is applied.

<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td></td><td></td><td>(3) When the FF key is pressed at FF.REW position, FF display is made and then the same brake release processing as (2) is taken.
(4) If the cassette is already inserted and end sensor="H" or start sensor="H" is present, the same brake release processing as (2) is taken.
(5) In tape slack detection, it takes such a brake release processing identical to (2).
(6) When the REW key is pressed in case of EE (L)="H" at PB.REC posi., VSR display is made and brake solenoid="H" made, shifting to the VSR position. After shifting, brake solenoid="L" is applied.
Then, when the VSR mode is released, it makes brake solenoid="H" after stopping of tape running, and then upon shifting to PB.REC position, brake solenoid="H" is made.
(7) In the item of (2), (3) and (4) of capstan UL, brake solenoid="L" is made immediately before capstan UL (L)="H".
(8) It makes brake solenoid="L" immediately before release of FF/REW.</td></tr>
<tr><td>52</td><td>LOADING RVS CTL</td><td>(1) It is an output terminal for controlling the rotating direction of loading motor.</td></tr>
<tr><td>53</td><td>LOADING FWD CTL</td><td>Given below is the relevant combination.
<table>
<tr><th>Control Signal / Mode</th><th>Loading motor positive-turn CTL</th><th>Loading motor reverse-turn CTL</th></tr>
<tr><td>Loading motor Stop</td><td>L</td><td>L</td></tr>
<tr><td>Loading motor positive-turn</td><td>H</td><td>L</td></tr>
<tr><td>Loading motor reverse-tur</td><td>H</td><td>H</td></tr>
</table>
Table 2-6.
(2) For stopping condition of mecha. actuation:
• Loading motor positive-turn CTL="L"
• Loading motor reverse-turn CTL="L"
(3) The following functions are provided so as to prevent any over-current to the loading motor.
• 2.0 sec. shut-off at cassette controller actuation
• 7.0 sec. shut-off at loading arm actuation
(4) For shut-off, there should be loading motor positive-turn CTL="L" and loading motor reverse-turn CTL="L", and the loading motor is stopped, and then stoppage is continued at that position until the operating key input has any change.
However, if during positive-turn of cassette controller, the motor is reversely turned and the cassette is ejected at once.
(5) Actuation of cassette controller
i) In cassette insertion, unless the cassette controller moves to the cassette controller down-posi. within 2 sec., it is actuated in Eject direction immediately, and further if not moved to the cassette controller up-posi. within 2 sec., it takes shut-off.
ii) For cassette controller Eject, unless the cassette controller moves to the cassette controller up-posi. within 2 sec., it is actuated in the cassette inserting direction, and if not moved to the cassette controller down-posi. within 2 sec., it takes shut-off.</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td>54</td><td>CAPSTAN UL (L)</td><td>A signal to control a reel rotating torque
(1) The capstan UL is a torque control voltage to be applied to the capstan motor, and to be "L" during unloading, at start of FF/REW or at tape-winding at Eject.
i) If the Stop/FF/REW mode is obtained at PB. REC position, the loading motor is reversely turned, and after about 500 msec., capstan UL (L)="L" is made, and the capstan motor is reversely turned, stopping the capstan motor and capstan UL (L)="H" at brake release position.
ii) When the FF key is pressed at FF. REW position, FF display is made, and after brake release, capstan UL (L)="L" is made, and the capstan motor is positive-turned and about 500 msec. later, capstan UL (L)="H" is applied.
iii) When the REW key is pressed at FF. REC position, REW display is made, and after brake release, capstan UL (L)="H" is made, and the capstan motor is reversely turned and about 500 msec. later, capstan UL (L)="H" is applied.
(2) In tape slack detection or leader tape-winding processing, for start of tape running, about 500 msec. capstan UL (L)="L" is to be applied. However, if the above processing is completed within 500 ms., capstan UL (L)="H" is made immediately.
(3) Idler move at start of loading action.
(4) Loose-tape winding processing upon cassette insertion (300 msec.)
(5) Loose-tape winding processing during Eject actuation.
(6) Countermeasure for tape slack at FF→Stop</td></tr>
<tr><td>55</td><td>CAPSTAN PU (L)</td><td>A signal to control a reel rotating torque
(1) The capstan PU is a signal for controlling the torque control voltage of capstan motor, and outputs at the following timing.
i) At transfer from PB. REC posi. to VSR posi.
ii) At return from VSR posi. to PB/REC posi.
iii) At idler move (Neck swing processing)
iv) Idler move from tape-winding upon cassette insertion
v) Idler move at REC—REC. Pause</td></tr>
<tr><td>56</td><td>CAPSTAN RVS (H)</td><td>It is a control signal for determining the rotating direction of capstan motor.
(1) The mode is made by combining the terminal ⑤⑦ with forced acceleration.
<table>
<tr><th>Control signal / Mode</th><th>Forced acceleration</th><th>Capstan motor reverse turn</th></tr>
<tr><td>Capstan motor stop</td><td>L</td><td>L</td></tr>
<tr><td>Capstan motor positive turn</td><td>H</td><td>L</td></tr>
<tr><td>Capstan motor reverse turn</td><td>H</td><td>H</td></tr>
</table>
Table 2-7.</td></tr>
<tr><td>57</td><td>CAPSTAN CTL
(Forced acceleration)</td><td>It is an output accelerating (stopping) the rotation speed to the capstan motor.
(1) For Slow/Still:
i) At Still (still image) replay→Forced acceleration="H"
ii) At Slow/Frame advance→Refer to a frame advance timing chart.
2) Other than Slow/Still
i) Capstan motor rotation: Forced acceleration="Z"
ii) Capstan motor stop: Forced acceleration="L"</td></tr>
</table>

Pin No.	Control Signal	Specifications
58	CURRENT LMT	It is an output offering a torque (current) limit to the capstan motor. (1) In case of Power CTL (L)="L", current limit="L" is outputted. (2) For Power CTL (L)="L": i) At Still (still image) replay→Current limit="Z" ii) At Slow/Frame advance→Refer to frame advance timing chart. iii) For other than above, current limit="H" is outputted.
59	DRUM CTL	This signal is to control the drum motor rotation, and stops the drum motor in case of drum mute (L)="L". (1) If PB, VSR, VSF, Still, Slow, double speed or REC display is obtained at FF/REW position, drum mute (L)="Z" is applied, and after 500 ms, loading is started. (2) If Stop, FF or REW is obtained at PB/REC position, unloading is started, and after completion, drum mute (L)="L" is applied. (3) Lateral swing acceleration at Slow/Still→Refer to a frame advance timing chart.
60	CTL GAIN SW (L)	It is a gain selecting output of PB-CTL amp. at FF/REW. (1) At FF/REW→CTL gain selecting CTL="H" output Other than above→CTL gain selecting CTL="L" output
61	X2 (H)	At double speed → "H" Not used
62	FV CTL	It is a control signal for APC correction of drum in trick mode. (1) In case of trick="H", drum correction is done. (2) At VS-F/R, double speed, slow & Still mode, trick="H" is made. (3) The timing of trick="L" is to be 1 sec. after phasing term after PB mode shifting.
63	FV	In trick mode (VS-F/R), it generates FV/FH and applies the synchronization. (1) Such a FV is generated in VS-F/R mode, mecha. shift time of PB→VS-R, mecha. shift time at VS-R release, mode holding time of VS-F/R release Slow/Still, and in the case of Head 2 giving no double speed. (2) The generation timing waveform is as shown below. (Note: H.SW.P applies to both rising and trailing.)  Note) M: High impedance Figure 2-15.

<table>
<tr><th>Pin No.</th><th>Control Signal</th><th>Specifications</th></tr>
<tr><td></td><td></td><td>(3) Modes and output waveforms are listed below
<table>
<tr><th rowspan="2">Mode</th><th rowspan="2">Recording Mode</th><th colspan="2">Head SW Pulse</th></tr>
<tr><th>Rising</th><th>Trailing</th></tr>
<tr><td rowspan="2">VS-Forward/Reverse</td><td rowspan="2">4-head (SP)
(LP)</td><td>B mode</td><td>B mode</td></tr>
<tr><td>D mode</td><td>D mode</td></tr>
<tr><td rowspan="2">Still/Slow</td><td rowspan="2">4-head (SP)
(LP)</td><td>A mode</td><td>B mode</td></tr>
<tr><td>D mode</td><td>C mode</td></tr>
<tr><td rowspan="2">Double Speed</td><td rowspan="2">4-head (SP)
(LP)</td><td>A mode</td><td>B mode</td></tr>
<tr><td>D mode</td><td>C mode</td></tr>
</table>
Table 2-8.</td></tr>
<tr><td>64</td><td>GND CTL</td><td>It controls the (−) terminal of CTL head.
(1) 100 ms after bias CTL (L)="L", it should be GND CTL="L". (At REC)
(2) It should be bias CTL (H)="H", together with GND CTL="H".
(3) Normally, it should be "H".</td></tr>
</table>

2-3. Data Transmission Specification of Mechanism Controller Corresponding to Serial Mode Servo

- Data is transmitted with the following format.

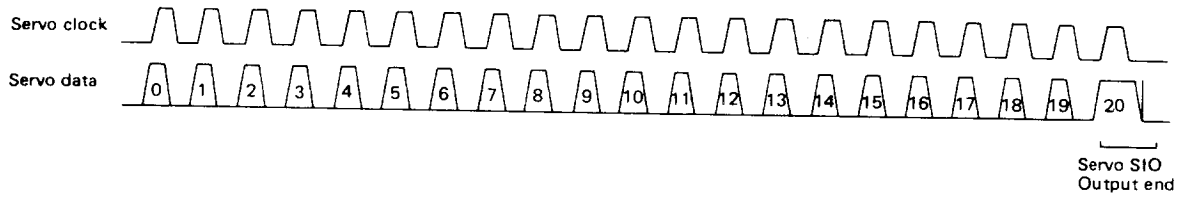


Figure 2-16.

(1) 21 bit data is outputted to the servo IC through the 2-line system consisting of servo clock (SCK) and servo data (SI).
(2) The servo data latches at the tail edge of servo clock. Servo SIO ends when the servo data is set to "H" at the servo clock tail.

1. Relation between Modes and Service Data

(The servo IC corresponds to RH-IX0431GEZZ)

Mode	Serial Data																
	0~5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
POWER OFF	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Serial transmission stop
POWER ON STOP	*1)	1	1	0	1	1	0	0	1	*2)		1	0	1	0	0	(FF2)
For 2.0S after FF start	*1)	1	1	0	1	1	0	0	0	*2)		1	0	0	1	0	(FF1)
FF subsequent	*1)	1	1	0	1	1	0	0	1	*2)		1	0	0	1	0	(FF2)
For 2.0S after REW start	*1)	1	1	1	1	1	0	0	0	*2)		1	0	0	1	0	(REW1)
REW subsequent	*1)	1	1	1	1	1	0	0	1	*2)		1	0	0	1	0	(REW2)
PB SP mode	*1)	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	(PB)
LP mode	*1)	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	(PB)
SP fixed mode	*1)	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	(PB)
VSF (M)	*1)	1	1	0	1	0	0	0	0	*2)		1	0	0	1	0	(SER2) SP: *5, LP: *5
(H)	*1)	1	1	0	1	0	0	1	0	*2)		1	0	0	1	0	(SER3) SP: *7, LP: *7
VSR (M)	*1)	1	1	1	1	0	0	0	0	*2)		1	0	0	1	0	(SER2/R) SP: *5, LP: *5
(H)	*1)	1	1	1	1	0	0	1	0	*2)		1	0	0	1	0	(SER3/R) SP: *7, LP: *7
SLOW	*1)	1	1	0	1	1	1	0	0	1	1	1	0	1	0	0	(SLOW)
STILL	*1)	1	1	0	0	0	0	0	0	1	1	1	0	1	0	0	(SLOW)
High speed	*1)	1	1	0	0	1	1	0	0	*2)		1	0	0	0	0	(*2)
REC SP mode	*1)	0	0	0	0	0	0	0	0	1	0	1	*3)	0	0	0	(REC)
LP mode	*1)	0	0	0	0	0	0	0	0	0	1	1	*3)	0	0	0	(REC)
SP fixed mode	*1)	0	0	0	0	0	0	0	0	0	0	1	*3)	0	0	0	(REC)
REC/pause	*1)	0	1	0	0	0	0	0	0	*2)		1	0	1	0	0	(REC · ASB)
Loading	*1)	0	1	0	0	0	0	0	0	*2)		1	0	1	0	0	(REC · ASB)
Unloading	*1)	1	1	0	1	1	0	0	1	*2)		1	0	0	0	0	(FF2)
Short loading	*1)	1	1	0	1	0	0	0	0	*2)		1	0	0	1	0	(SER1) / (*2)
Short unloading	*1)	1	1	0	0	0	0	0	0	*2)		1	0	1	0	0	(PB)
Trick cancel	*1)	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	(PB)
Short rewinding	*1)	0	1	0	0	0	0	0	0	*2)		1	0	0	0	0	(REC · ASB)
Phase matching	*1)	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	(REC · ASB)

Note *1 : Tracking delay time
D0 to D5 = "1 0 0 0 0 0" only in REC mode
In other modes the preceding data remains.

Note *2 : SP : 1 0
LP : 0 1
SP fixed : 0 0
Holding : 1 1

Note *3 : Only when writing the VISS signal: "1"
In other cases: "0"

Table 2-9.

2. Serial data D0 to D5

Serial Data						Tracking Delay time (msec)
0	1	2	3	4	5	
0	0	0	0	0	0	5.22
		↓				↓
0	1	1	1	0	1	18.62
		↓				↓
1	0	0	0	0	0	20.00
		↓				↓
1	1	1	0	1	0	32.01
		↓				↓
1	1	1	1	1	1	34.32

Note: The output from pin (31) of the servo IC (RH-IX0431GEZZ) is delayed by 5.22 msec.

Table 2-10.

3. Serial data D14 to D15

Serial Data		Speed Data
14	15	
1	0	SP
0	1	LP
0	0	SP fixed
1	1	Holding

Table 2-11.

4. Serial data D16 to D20

D16	Head Selection
0	D/A 4 Head
1	2 Head

D17	REC / DUTY Selection
0	REC · CTL 27.5%
1	REC · CTL 60 %

D18	CAP / SERVO SW
0	ANALOG SW ON
1	ANALOG SW OFF

D19	Hysteresis Width
0	300mVpp
1	600mVpp

D20	REC / CTL Selection
0	High-Z
1	GND

Table 2-12.

3-4. Serial Transmission Format between System Controller and Timer

1. Format of Data Transmitted from System Controller to Timer

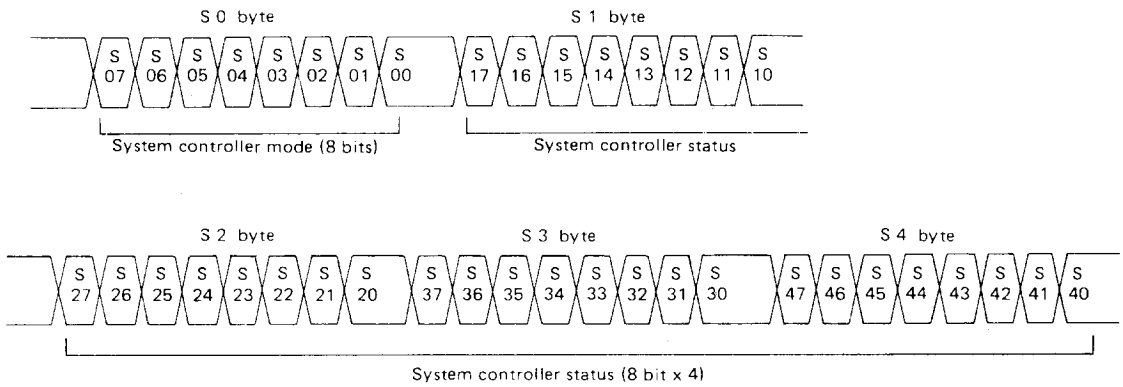


Figure 2-17.

(1) 5-byte data is transmitted by one transmission sequence.
(2) The S0 byte is arranged so that 8 bits compose one system controller mode data.
(3) The system controller mode is the system controller operation modes.
(4) The S1, S2, S3 and S4 bytes are 8 bite data which are used as system controller status data.
(5) The content of system controller status is represented the status of pertinent sensor by each bit.
(6) The timer makes the data valid when the same data is received twice successively (for S0, S1, S2, S3, S4).

2. Format of Data Transmitted from Timer to System Controller

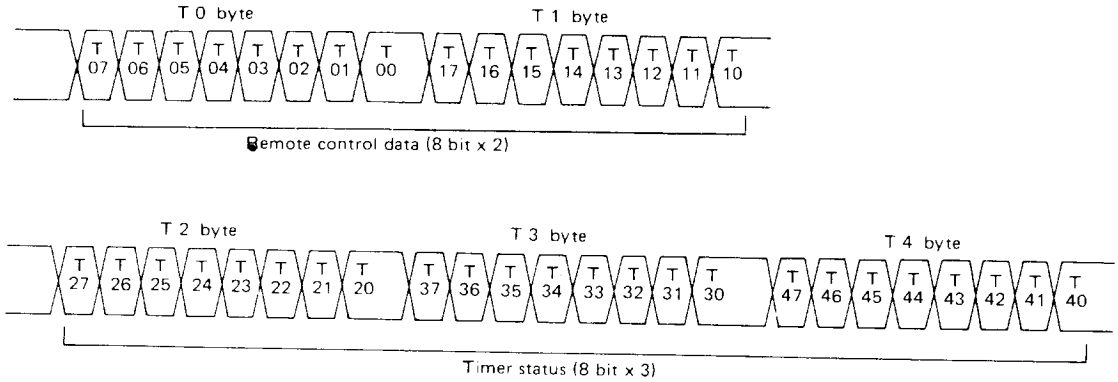
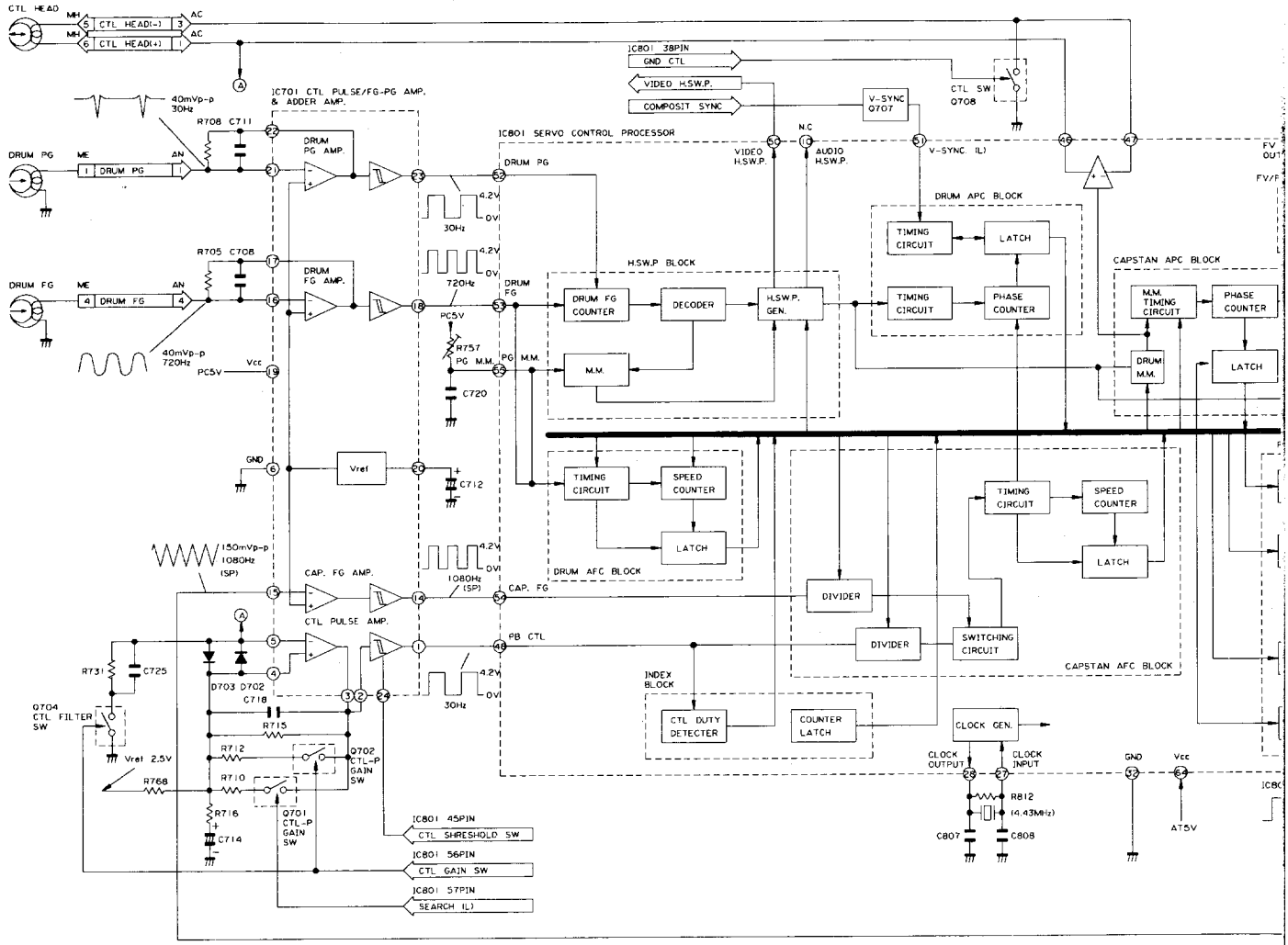


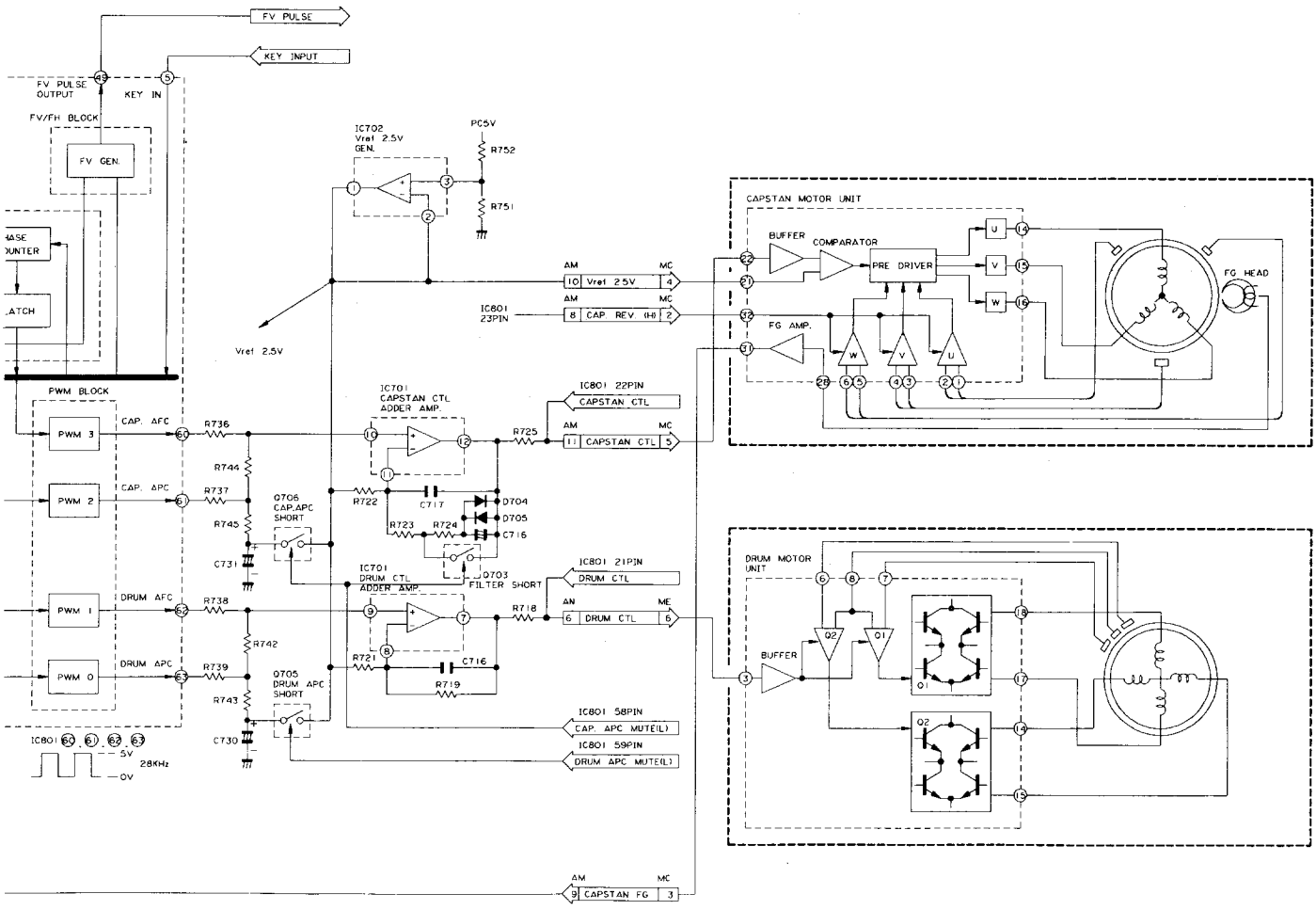
Figure 2-18.

(1) 5-byte data is transmitted by one transmission sequence.
(2) T0 byte and T1 byte are 8 bit data which are used as remote control data.
(3) The remote control data and they are determined by the content of control signals from the optical remote control and timer.
(4) The T0 byte and T1 byte have always the same data content.
(5) The system controller makes the remote control data valid if the T0 byte and T1 byte match with each other.
(6) The T2, T3 and T4 bytes are time master status data. The timer status consists of 8-bit flag it represents the timer status.
(7) The system controller makes the timer status data valid when the same timer status data is received twice successively.

Servo Process Block Diagram
(FOR 2-HEAD MODELS): VC-A10 SERIES



Figu


FV PULSE
KEY INPUT
FV PULSE OUTPUT
KEY IN
FV/FH BLOCK
FV GEN.
IC702 Vref 2.5V GEN.
PC5V
R752
R751
Vref 2.5V
CAPSTAN MOTOR UNIT
BUFFER
COMPARATOR
PRE DRIVER
FG AMP.
FG HEAD
IC801 23PIN
AM
MC
10 Vref 2.5V 4
8 CAP. REV. (H) 2
PWM BLOCK
PWM 3
PWM 2
PWM 1
PWM 0
CAP. AFC
CAP. APC
DRUM AFC
DRUM APC
R736
R737
R738
R739
R744
R745
R742
R743
C731
C730
IC701 CAPSTAN CTL ADDER AMP.
R722
C717
R723
R724
D704
D705
C716
Q706 CAP.APC SHORT
Q703 FILTER SHORT
R725
IC801 22PIN
CAPSTAN CTL
11 CAPSTAN CTL 5
IC701 DRUM CTL ADDER AMP.
R721
R719
R718
Q705 DRUM APC SHORT
IC801 21PIN
DRUM CTL
AN
ME
6 DRUM CTL 6
DRUM MOTOR UNIT
Q1
Q2
IC801 58PIN
CAP. APC MUTE(L)
IC801 59PIN
DRUM APC MUTE(L)
IC801 60, 61, 62, 63
5V
0V
28KHz
9 CAPSTAN FG 3

Servo Process Block Diagram
(FOR 2-HEAD MODELS): VC-A30/A35/A40/A45 SERIES

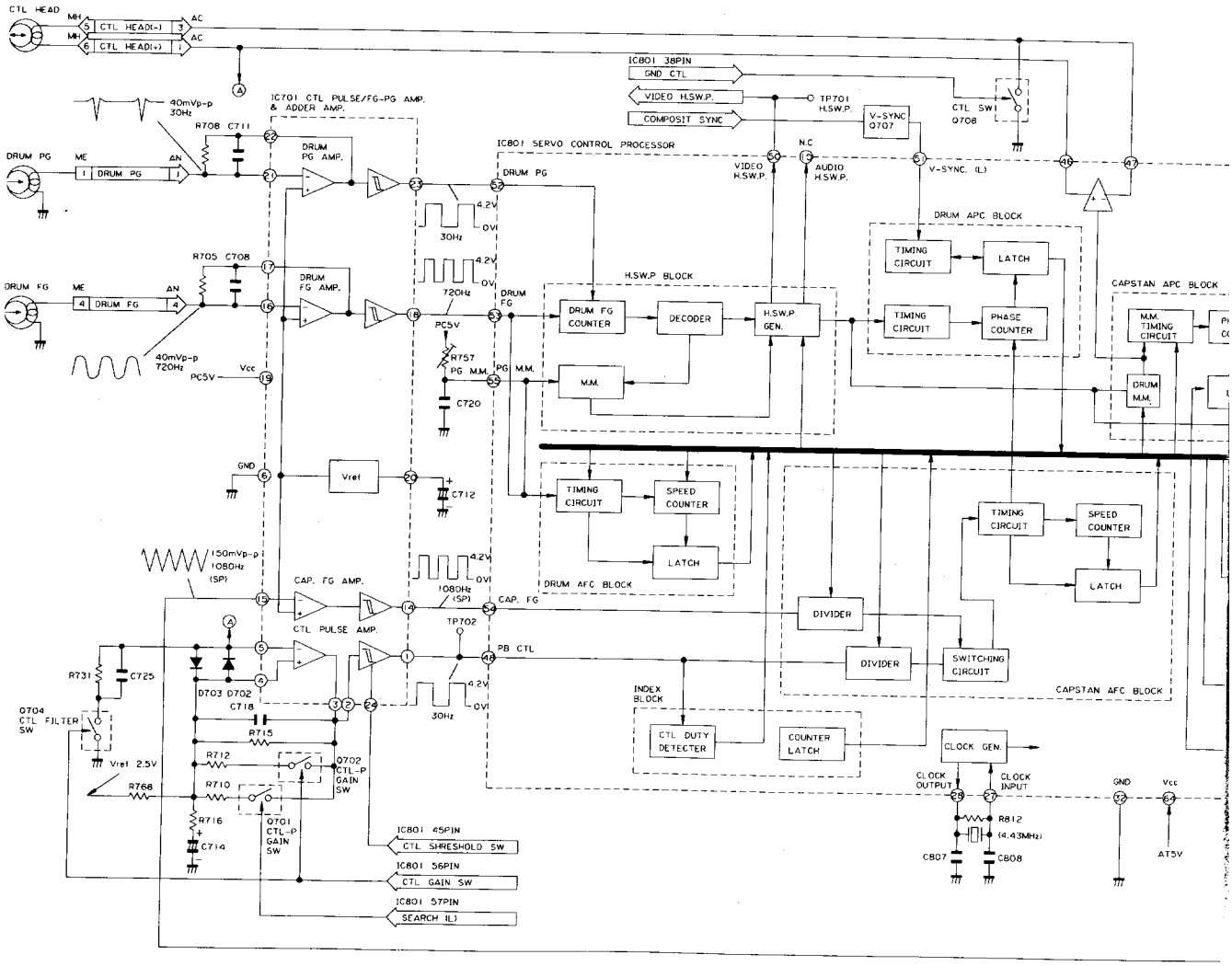
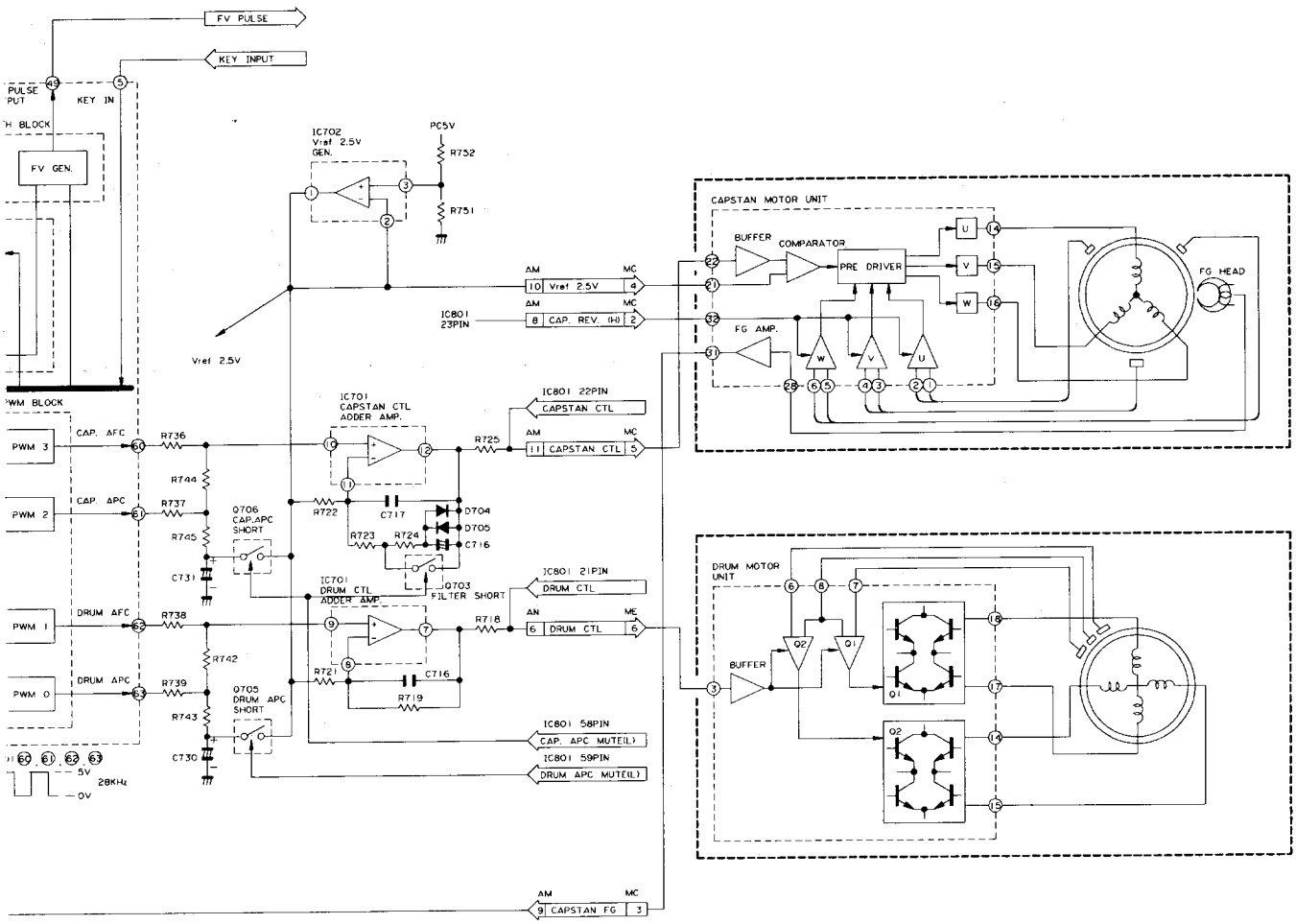
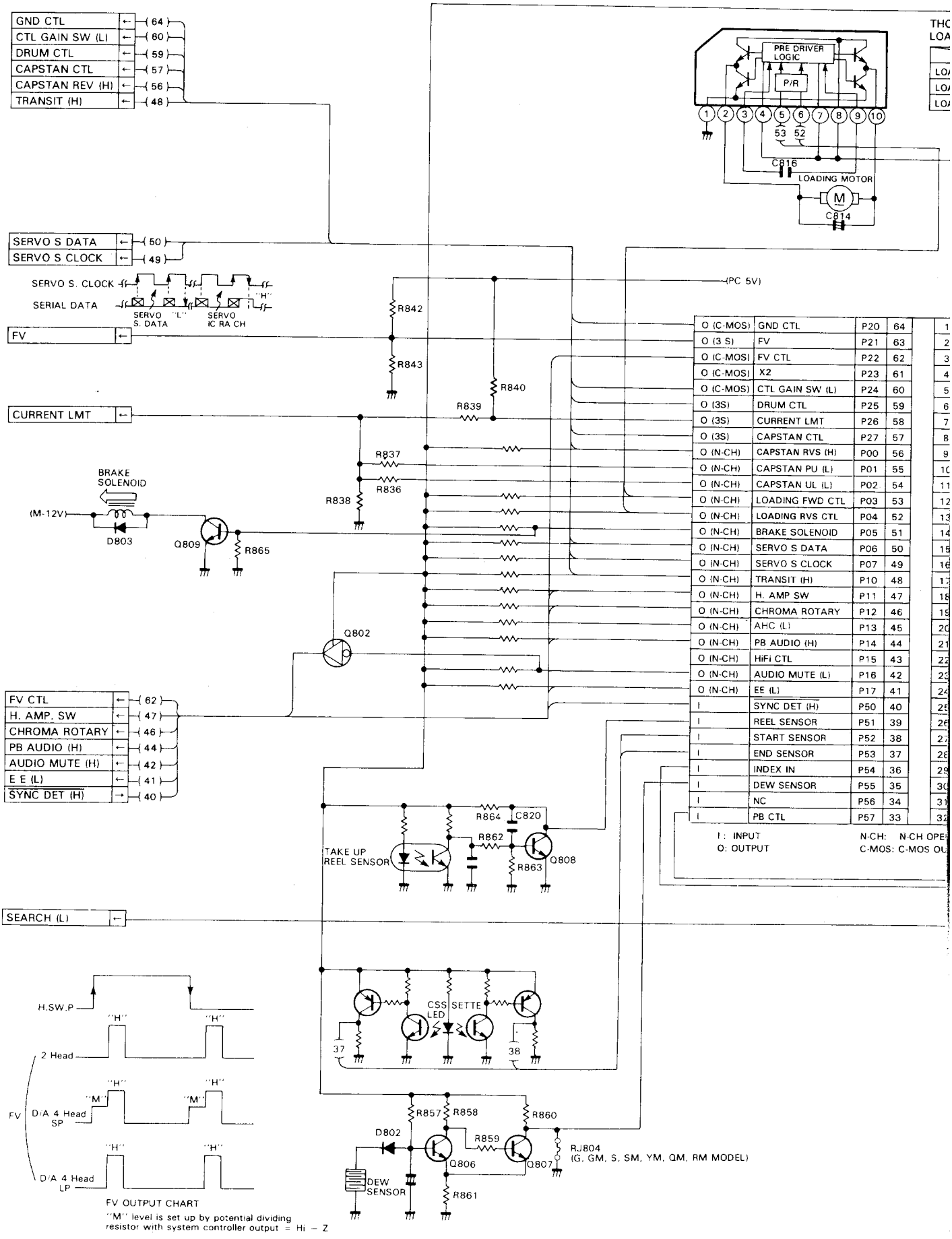


Figure 2-19.


F.V PULSE
KEY INPUT
PULSE PUT
KEY IN
H BLOCK
F.V GEN.
IC702 Vref 2.5V GEN.
PC5V
R752
R751
Vref 2.5V
CAPSTAN MOTOR UNIT
BUFFER
COMPARATOR
PRE DRIVER
FG AMP.
FG HEAD
U
V
W
AM MC
10 Vref 2.5V 4
IC801 23PIN
8 CAP. REV. (H) 2
PWM BLOCK
PWM 3
CAP. AFC
R736
IC701 CAPSTAN CTL ADDER AMP.
IC801 22PIN
CAPSTAN CTL
R725
11 CAPSTAN CTL 5
R744
PWM 2
CAP. APC
R737
R745
Q706 CAP.APC SHORT
R722
C717
D704
D705
C716
R723
R724
C731
IC701 DRUM CTL ADDER AMP.
Q703 FILTER SHORT
IC801 21PIN
DRUM CTL
PWM 1
DRUM AFC
R738
R718
AN ME
6 DRUM CTL 6
R742
PWM 0
DRUM APC
R739
R743
Q705 DRUM APC SHORT
R721
C716
R719
C730
5V
0V
28KHz
IC801 58PIN
CAP. APC MUTE(L)
IC801 59PIN
DRUM APC MUTE(L)
DRUM MOTOR UNIT
BUFFER
Q2
Q1
9 CAPSTAN FG 3

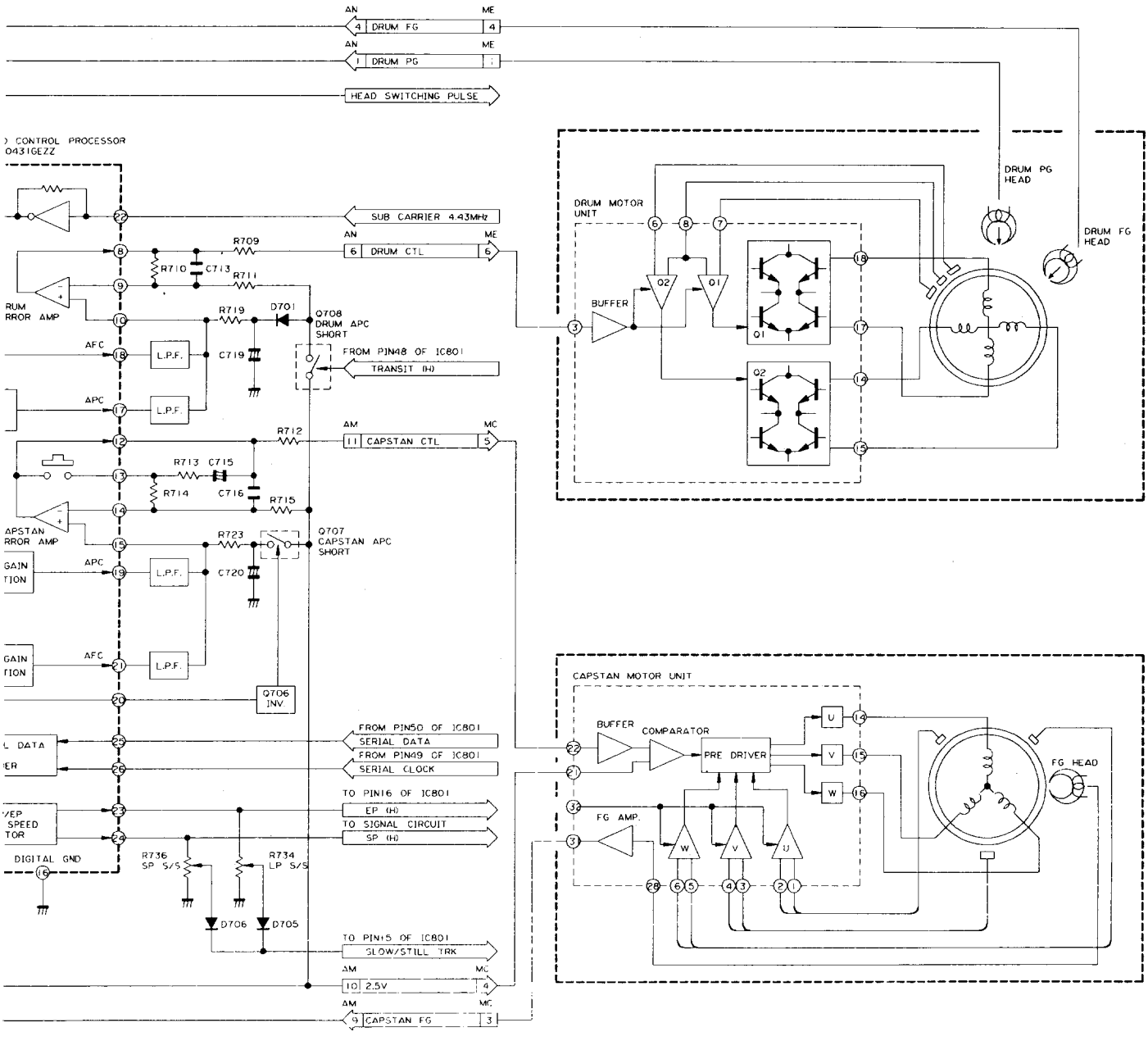
ıre 2-20.

System Controller Block Diagram



O (C-MOS)	GND CTL	P20	64	1
O (3 S)	FV	P21	63	2
O (C-MOS)	FV CTL	P22	62	3
O (C-MOS)	X2	P23	61	4
O (C-MOS)	CTL GAIN SW (L)	P24	60	5
O (3S)	DRUM CTL	P25	59	6
O (3S)	CURRENT LMT	P26	58	7
O (3S)	CAPSTAN CTL	P27	57	8
O (N-CH)	CAPSTAN RVS (H)	P00	56	9
O (N-CH)	CAPSTAN PU (L)	P01	55	10
O (N-CH)	CAPSTAN UL (L)	P02	54	11
O (N-CH)	LOADING FWD CTL	P03	53	12
O (N-CH)	LOADING RVS CTL	P04	52	13
O (N-CH)	BRAKE SOLENOID	P05	51	14
O (N-CH)	SERVO S DATA	P06	50	15
O (N-CH)	SERVO S CLOCK	P07	49	16
O (N-CH)	TRANSIT (H)	P10	48	17
O (N-CH)	H. AMP SW	P11	47	18
O (N-CH)	CHROMA ROTARY	P12	46	19
O (N-CH)	AHC (L)	P13	45	20
O (N-CH)	PB AUDIO (H)	P14	44	21
O (N-CH)	HiFi CTL	P15	43	22
O (N-CH)	AUDIO MUTE (L)	P16	42	23
O (N-CH)	EE (L)	P17	41	24
I	SYNC DET (H)	P50	40	25
I	REEL SENSOR	P51	39	26
I	START SENSOR	P52	38	27
I	END SENSOR	P53	37	28
I	INDEX IN	P54	36	29
I	DEW SENSOR	P55	35	30
I	NC	P56	34	31
I	PB CTL	P57	33	32

I : INPUT
O: OUTPUT
N-CH: N-CH OPE
C-MOS: C-MOS OU


AN
ME
4 DRUM FG 4
AN
ME
1 DRUM PG
HEAD SWITCHING PULSE
CONTROL PROCESSOR
0431GEZZ
SUB CARRIER 4.43MHz
AN
ME
6 DRUM CTL 6
R709
R710
C713
R711
D701
Q708
DRUM APC
SHORT
FROM PIN48 OF IC801
TRANSIT (H)
AFC
APC
L.P.F.
C719
R712
AM
MC
11 CAPSTAN CTL 5
R713
C715
R714
C716
R715
Q707
CAPSTAN APC
SHORT
R723
C720
Q706
INV
FROM PIN50 OF IC801
SERIAL DATA
FROM PIN49 OF IC801
SERIAL CLOCK
TO PIN16 OF IC801
FG (H)
TO SIGNAL CIRCUIT
SP (H)
DIGITAL GND
R736
SP S/S
R734
LP S/S
D706
D705
TO PIN15 OF IC801
SLOW/STILL TRK
10 2.5V 4
9 CAPSTAN FG 3
DRUM MOTOR
UNIT
BUFFER
Q2
Q1
DRUM PG
HEAD
DRUM FG
HEAD
CAPSTAN MOTOR UNIT
BUFFER
COMPARATOR
PRE DRIVER
FG AMP.
FG HEAD
U
V
W

Servo Process Block Diagram
(FOR 4-HEAD MODELS): VC-A50/A60/A61/A62 SERIES

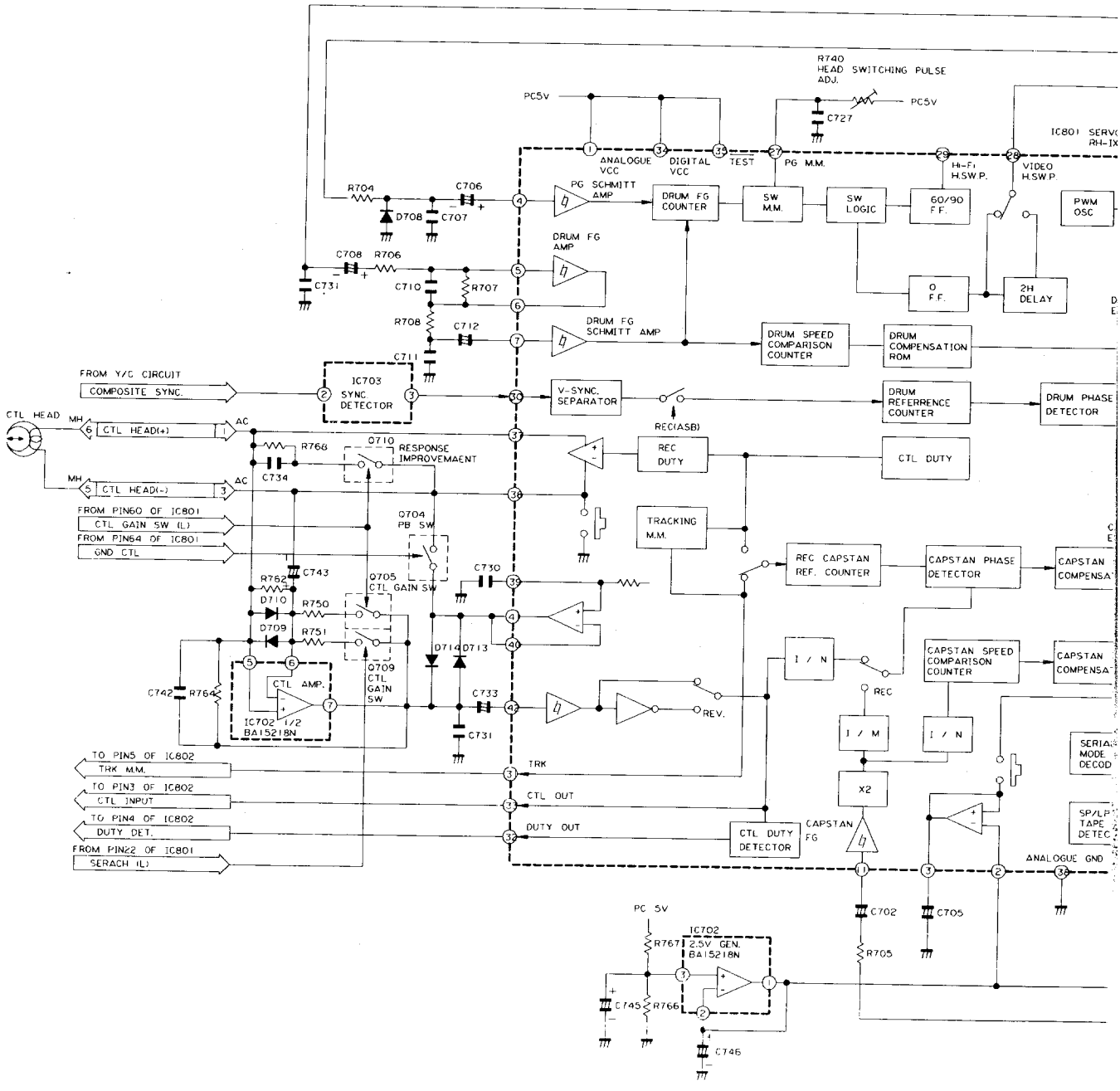


Figure 2-21.

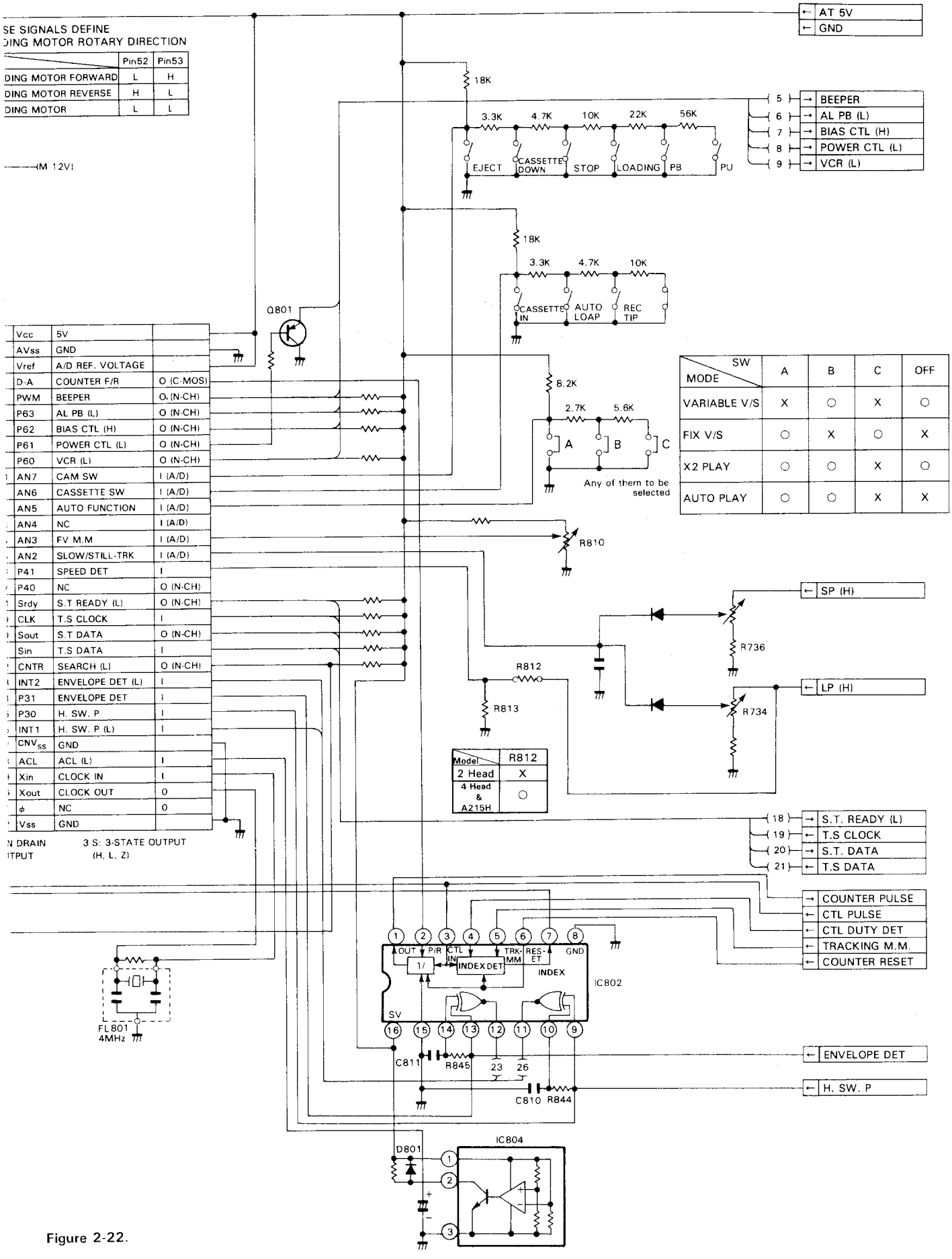

SE SIGNALS DEFINE
DING MOTOR ROTARY DIRECTION
Pin52 Pin53
DING MOTOR FORWARD L H
DING MOTOR REVERSE H L
DING MOTOR L L
(M 12V)
AT 5V
GND
18K
3.3K 4.7K 10K 22K 56K
EJECT CASSETTE DOWN STOP LOADING PB PU
5 BEEPER
6 AL PB (L)
7 BIAS CTL (H)
8 POWER CTL (L)
9 VCR (L)
18K
3.3K 4.7K 10K
CASSETTE IN AUTO LOAP REC TIP
Q801
8.2K
2.7K 5.6K
A B C
Any of them to be selected
SW / MODE A B C OFF
VARIABLE V/S X ○ X ○
FIX V/S ○ X ○ X
X2 PLAY ○ ○ X ○
AUTO PLAY ○ ○ X X
R810
SP (H)
R736
R812
R813
LP (H)
R734
Model R812
2 Head X
4 Head & A215H ○
Vcc 5V
AVss GND
Vref A/D REF. VOLTAGE
D-A COUNTER F/R O (C-MOS)
PWM BEEPER O (N-CH)
P63 AL PB (L) O (N-CH)
P62 BIAS CTL (H) O (N-CH)
P61 POWER CTL (L) O (N-CH)
P60 VCR (L) O (N-CH)
AN7 CAM SW I (A/D)
AN6 CASSETTE SW I (A/D)
AN5 AUTO FUNCTION I (A/D)
AN4 NC I (A/D)
AN3 FV M.M I (A/D)
AN2 SLOW/STILL-TRK I (A/D)
P41 SPEED DET I
P40 NC O (N-CH)
Srdy S.T READY (L) O (N-CH)
CLK T.S CLOCK I
Sout S.T DATA O (N-CH)
Sin T.S DATA I
CNTR SEARCH (L) O (N-CH)
INT2 ENVELOPE DET (L) I
P31 ENVELOPE DET I
P30 H. SW. P I
INT1 H. SW. P (L) I
CNVss GND
ACL ACL (L) I
Xin CLOCK IN I
Xout CLOCK OUT O
ϕ NC O
Vss GND
N DRAIN 3 S: 3-STATE OUTPUT
ITPUT (H, L, Z)
18 S.T. READY (L)
19 T.S CLOCK
20 S.T. DATA
21 T.S DATA
COUNTER PULSE
CTL PULSE
CTL DUTY DET
TRACKING M.M.
COUNTER RESET
OUT P/R CTL IN INDEX DET TRK-MM RES-ET GND
INDEX
IC802
SV
FL801
4MHz
C811 R845 23 26
C810 R844
ENVELOPE DET
H. SW. P
D801
IC804

Figure 2-22.

3. TIMING CHART

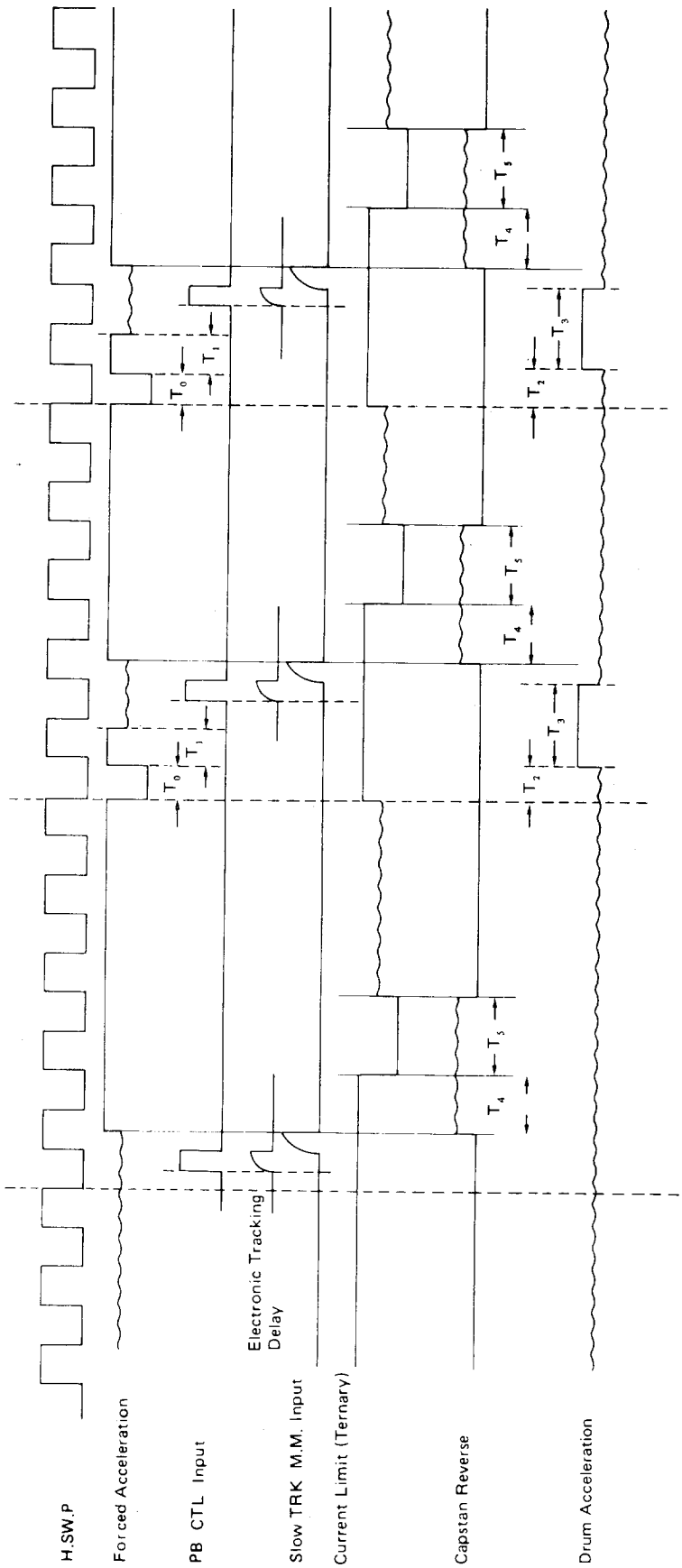


Figure 3-1.

Slow/Still Frame Advance Timing Chart (2-head system)

Symbol		Item	Preset Value		
			SP	LP	
Frame Advancing	T0	Start M/M	13.8 ms	—	
	T1	Forced acceleration M/M	16.6 ms	—	
	T2	Lateral swing acceleration start time	18.7 ms	—	
	T3	Lateral swing acceleration M/M	45.8 ms	—	
	T4	Speed reduction M/M	12.0 ms	—	
	T5	Brake M/M	13.6 ms	—	
	T6	———	—	—	
	T7	———	—	—	
Release	T8	Forced acceleration release	23.0 ms	—	
	T9	———	—	—	

Note: Head 2 is special for SP; therefore, Slow/Still M/M, etc. of LP is under study.

Table 3-1.

Slow/Still Frame Advance Timing Chart (4-head system)

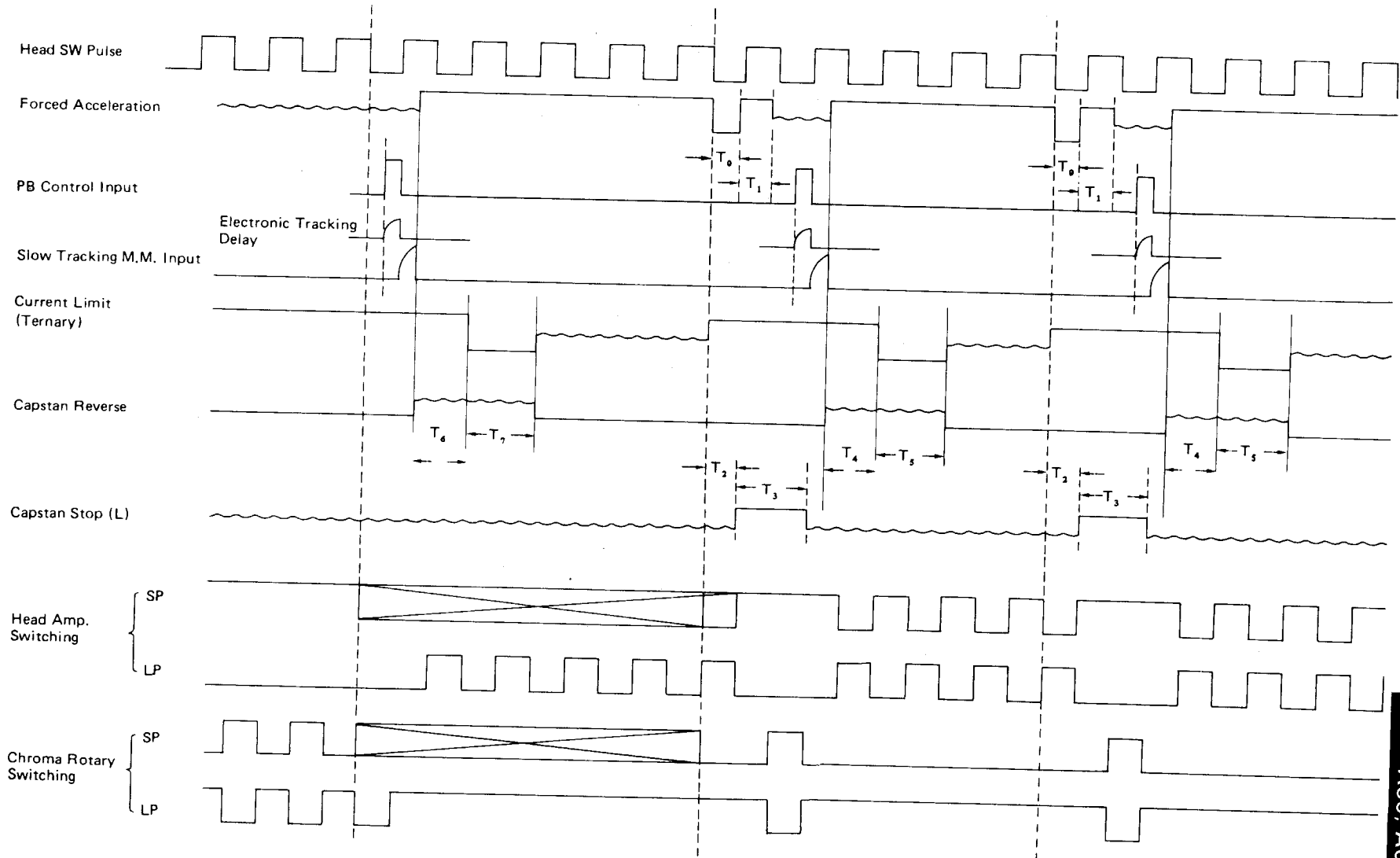


Figure 3-2.

Shift to PB mode when the SP Slow/Still mode is cleared

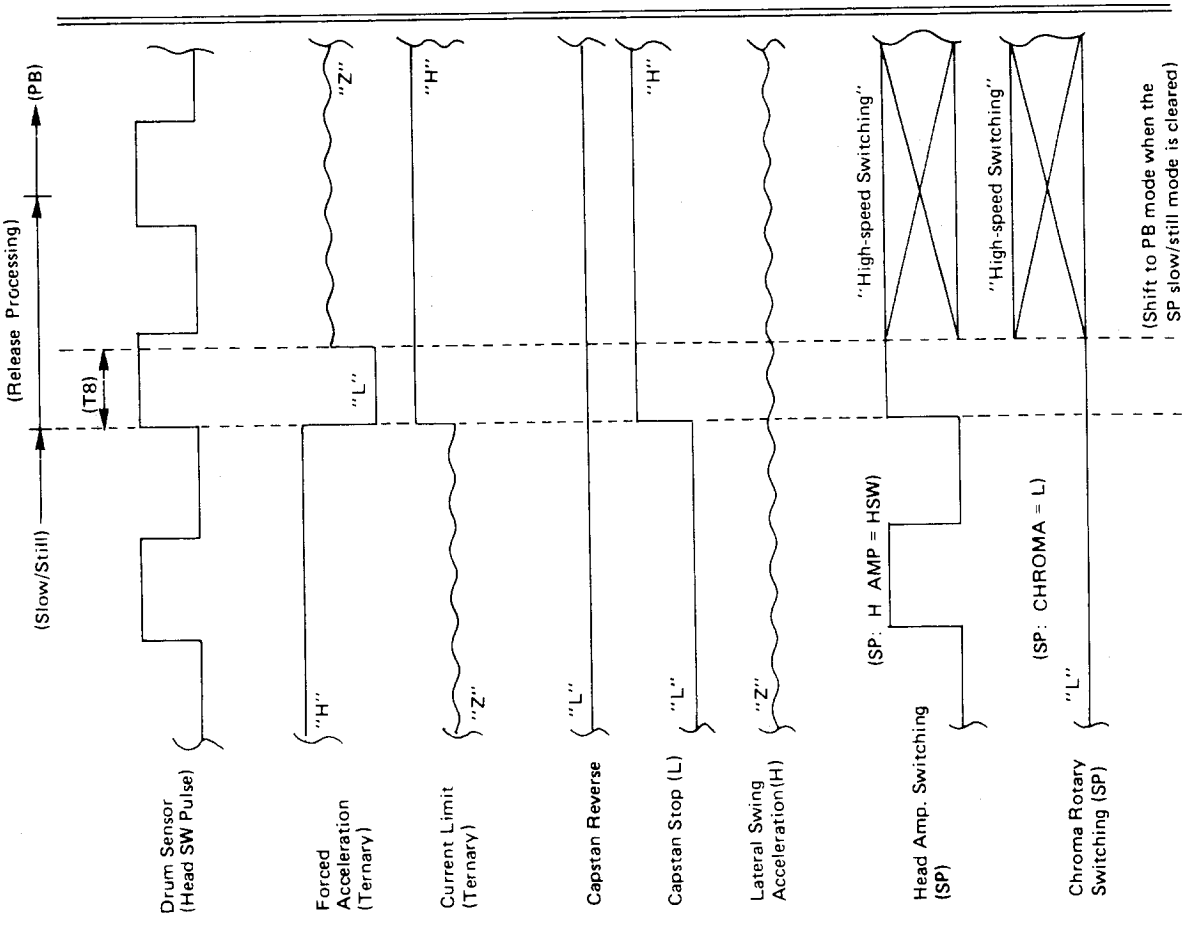


Figure 3-3.

Shift to PB mode when the LP Slow/Still mode is cleared

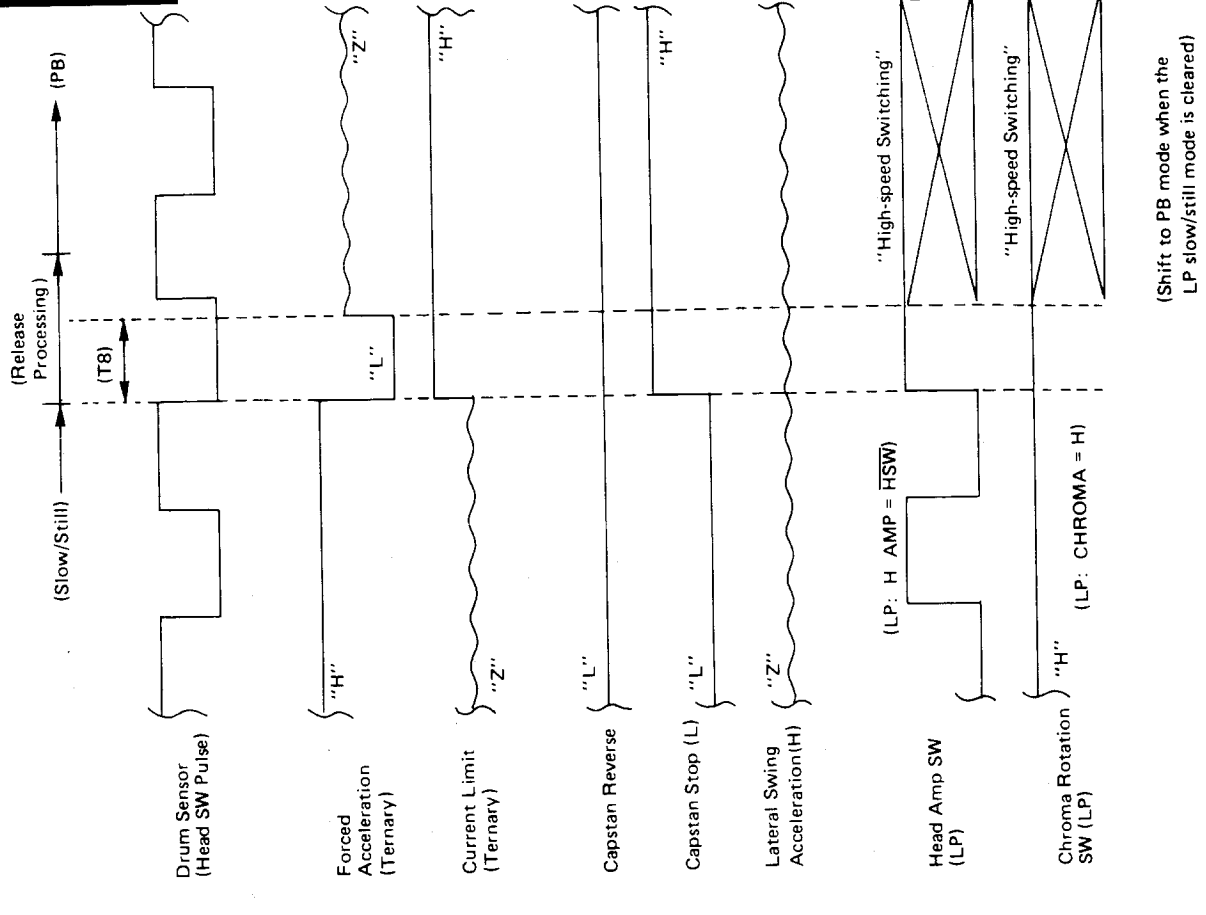


Figure 3-4.

Shift to REC/STOP mode when the SP Slow/Still mode is cleared

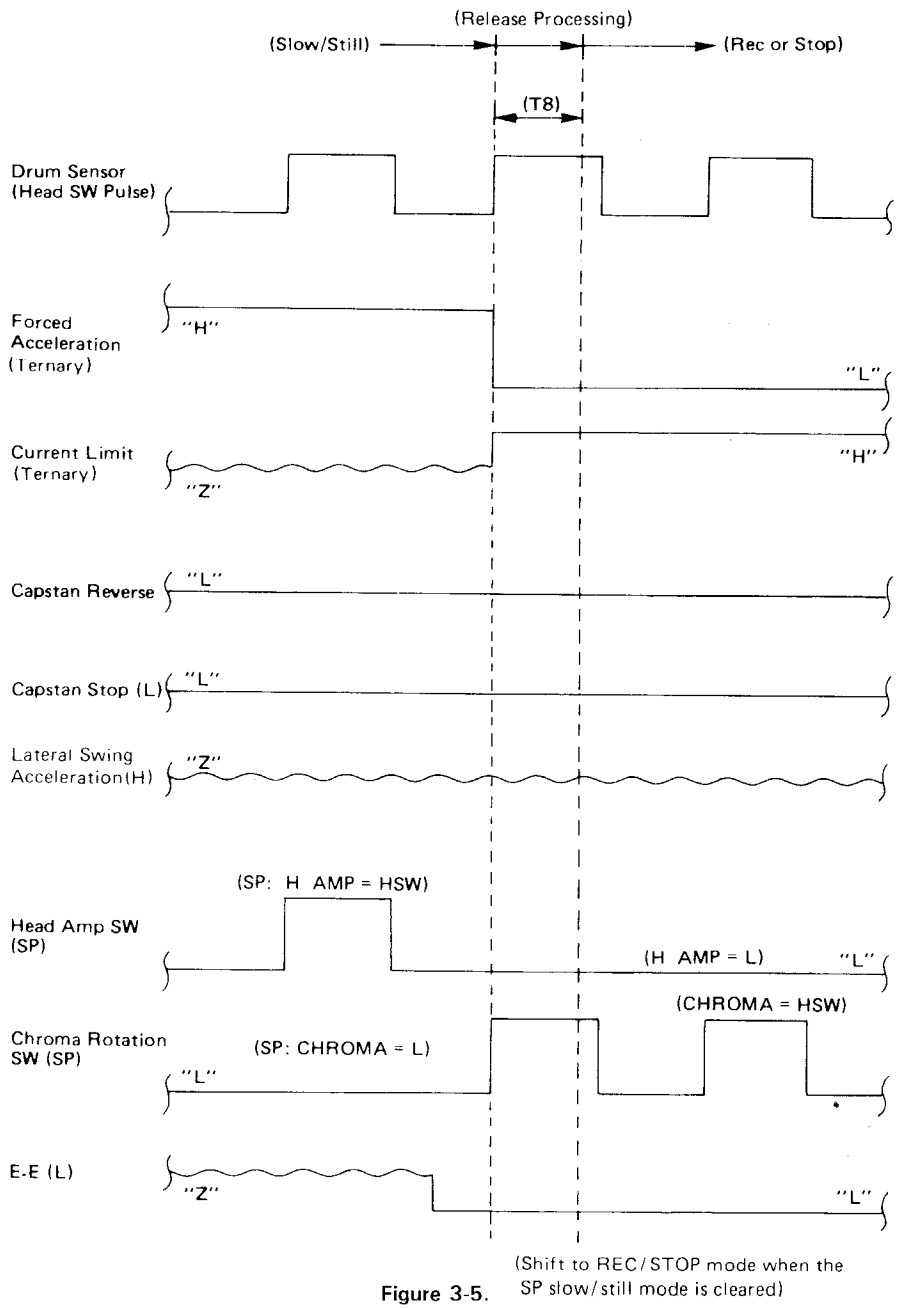


Figure 3-5.

Shift to REC/STOP mode when the LP Slow/Still mode is cleared

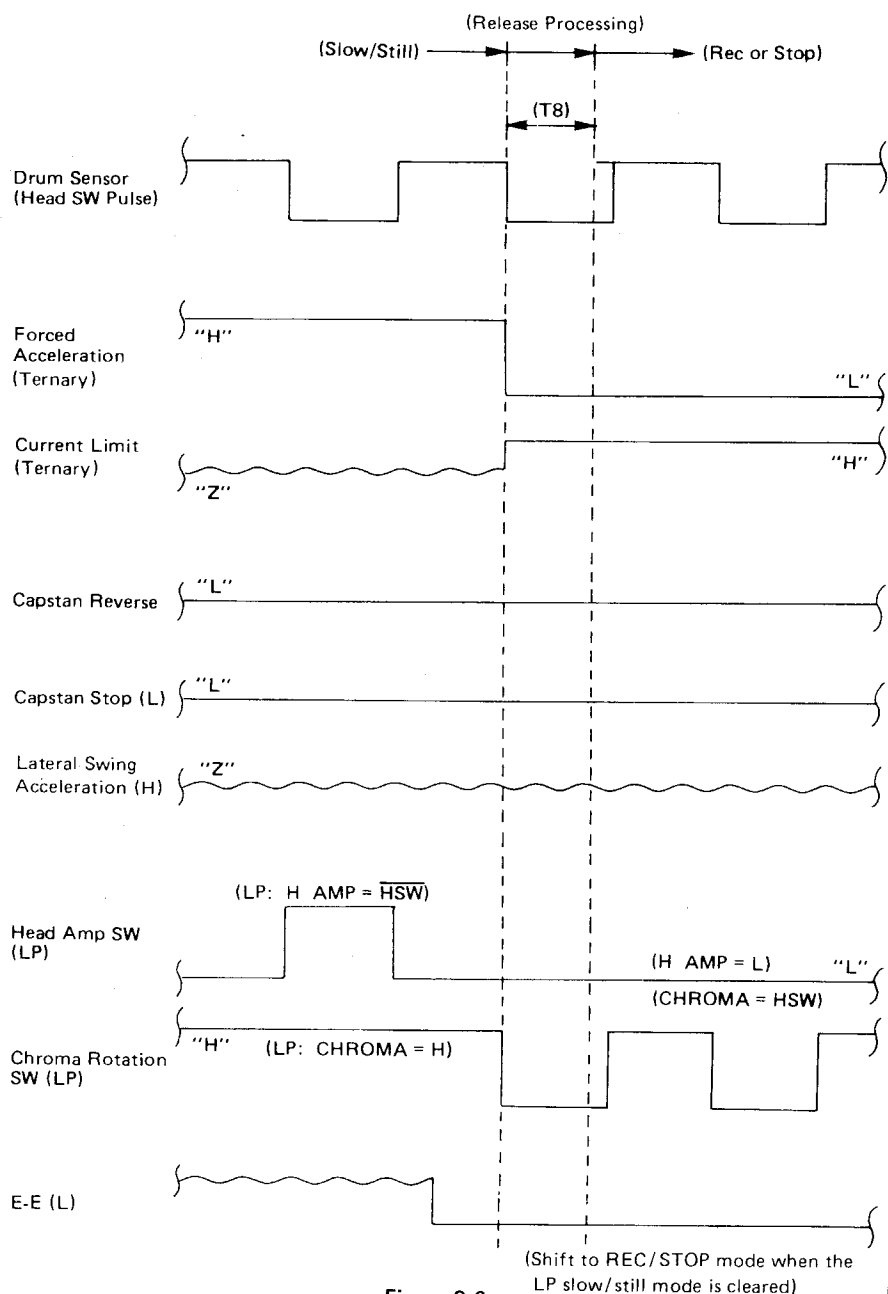


Figure 3-6.

Symbol		Item	Preset Value		
			SP	LP	
Frame Advancing	T0	Start M/M	14.08 ms	9.73 ms	
	T1	Forced acceleration M/M	18.94 ms	11.01 ms	
	T2	Lateral swing acceleration start time	23.04 ms	19.46 ms	
	T3	Lateral swing acceleration M/M	23.81 ms	33.28 ms	
	T4	Speed reduction M/M	11.78 ms	5.12 ms	
	T5	Brake M/M	12.29 ms	3.58 ms	
	T6	Speed reduction M/M (At Still On)	11.78 ms	7.94 ms	
	T7	Brake M/M (At Still On)	12.29 ms	3.58 ms	
Release	T8	Forced acceleration release	23.04 ms	9.22 ms	
	T9	———	—	—	

Note: Head 2 is special for SP; therefore, Slow/Still M/M, etc. of LP is under study.

Table 3-2.

4. TIMER CIRCUIT RH-IX0581GEZZ (VC-A60X, NZ, WT, VC-A61T, VC-A62DT)

4-1. PIN ASSIGNMENT AND FUNCTIONAL DESCRIPTION OF EACH PIN

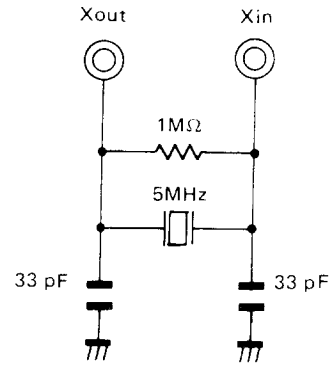
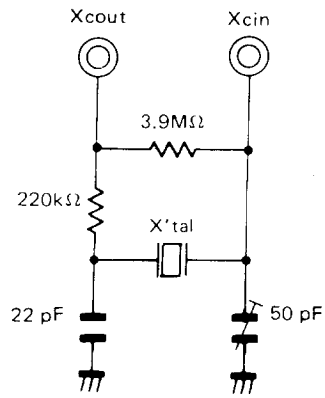
(1) Pin Assignment

Terminal Name	No.	Name		Name	No.	Terminal Name
G11	64	P40		Vcc	1	+5V
G10	63	P41		P65	2	AUDIO OUTPUT CTL
G9	62	P42		P64	3	E^2 PROM CS
G8	61	P43		P63	4	E^2 PROM CLK
G7	60	P44		P62	5	E^2 PROM SO/S1/OSD SO
G6	59	P45		P61	6	PWM OUTPUT
G5	58	P46		P60	7	AFT MUTE
G4	57	P47		P27	8	B0
G3	56	P00		P26	9	B1
G2	55	P01		P25	10	OSD MUTE/BLUE BACK
G1	54	P02		P24	11	OSD CLK
S13	53	P03		P23	12	OSD CS-(L)
S12	52	P04		P22	13	CTL FREQ. DIV. IC RESET
S11	51	P05		P21	14	SECAM OSD PROHIBIT INPUT
S10	50	P06	RH-iX0581GEZZ	P20	15	NORMAL (L)
S9	49	P07		Srdy	16	SYSCON READY-(L)
S4	48	P10		CLK	17	SYSCON/TIMER CLK
S5	47	P11		Sout	18	TIMER SERIAL DATA
S3	46	P12		Sin	19	SYSCON SERIAL DATA
S7	45	P13		P33	20	CTL PULSE (1/25)
S6	44	P14		P32	21	INTERNAL COUNTER CLK INPUT
S2	43	P15		P31	22	VIDEO TUNER (H)
S1	42	P16		P30	23	AUDIO TUNER (H)
S8	41	P17		INT1	24	A/C PULSE
NC	40	P50		INT2	25	R/C PULSE INPUT
PAY (H)	39	P51		CNV_{ss}	26	GND
−30V	38	Vp		RESET	27	RESET -(L)
KEY INPUT 1	37	P54		Xin	28	CLOCK INPUT
KEY INPUT 2	36	P55		Xout	29	CLOCK OUTPUT
KEY INPUT 3	35	P56		XCin	30	CLOCK INPUT FOR TIMER
KEY INPUT 4	34	P57		XCout	31	CLOCK OUTPUT FOR TIMER
X'TAL ADJ.	33	ϕ		V_{ss}	32	GND

Figure 4-1.

(2) Functional Description of Each Pin

Pin No.	Name	Description	I/O (Type)
1	Vcc	At 5V to be connected.	
2	AUDIO OUTPUT CTL	Control signal to switch the audio output between (L+R), L, R and NORMAL.	O (C-MOS)
3	E^2PROM CS	Used for serial transfer between Timer and E^2PROM. Note that pin No. 5 (E^2PROM SI/SO/OSD SO) is commonly used as the OSD Control serial port.	O (C-MOS)
4	E^2PROM CLK		O (C-MOS)
5	OSD SO/E^2PROM SI/SO		I/O (C-MOS)
6	PWM OUTPUT	Tuning voltage PWM output. 14-bit resolution.	O (C-MOS)
7	AFT MUTE	Output when the volsyn is in preset mode or when tuning is being done.	O (C-MOS)
8	B0	Band switching output for tuning	O (N-CH)
9	B1		O (N-CH)
10	OSD MUTE/ BLUE BACK	OSD control serial terminal.	O (N-CH) O (N-CH)
11	OSD CLK		O (N-CH)
12	OSD CS-(L)		O (N-CH)
13	CTL FREQ. DIV. IC RESET	Control signal to reset the CTL frequency dividing IC.	O (N-CH)
14	SECAM OSD PROHIBIT INPUT	Control signal to prohibit the superimpose function while receiving SECAM signal.	I
15	NORMAL (L)	Terminal commonly used for forced normal (L) output and LR display mute (L) input. (A mute signal is supplied via the N-CH open drain circuit. On Hi-Fi models.)	O (N-CH)
16	SYSCON READY-(L)	Control signal for serial transfer between timer and system controller.	I
17	SYSCON/TIMER CLK		O (N-CH)
18	TIMER SERIAL DATA		O (N-CH)
19	SYSCON SERIAL DATA		I
20	CTL PULSE (1/25)	1-second count source input for the real time counter.	I
21	INTERNAL COUNTER CLK INPUT	Clock count input for the timer. Connected to Pin No. 31. Shortest pattern possible to be taken for connection.	I
22	VIDEO TUNER (H)	Input switching control terminal.	O (N-CH)
23	AUDIO TUNER (H)		O (N-CH)

Pin No.	Name	Description	I/O (Type)
24	A/C PULSE	A/C-shaped signal input for power failure detection. Power failure is identified if there is no change in A/C pulse for 35 msec. External interrupt at the rising edge.	I
25	R/C PULSE INPUT	Rising edge of R/C pulse is detected. External interrupt at the rising edge to measure the interval between two rising edges of R/C pulse.	I
26	CNVss	Connected to GND (0V).	
27	RESET-(L)	All Clear is made when a voltage lower than 0.6V has been put in for 2 μsec or more after the supply voltage reached the microcomputer's operating voltage (5V ± 10%).	I
28 29	CLOCK INPUT CLOCK OUTPUT	System clock generating circuit built-in. System clock is obtained by adding a ceramic resonance circuit as shown below.  **Figure 4-2.**	I O
30 31	CLOCK INPUT FOR TIMER CLOCK OUTPUT FOR TIMER	Timer count clock generating circuit built-in. Timer count clock is obtained by adding a crystal resonance circuit as shown below.  **Figure 4-3.**	I O
32	Vss	Connected to GND (0V).	

Pin No.	Name	Description	I/O (Type)
33	X'tal ADJ.	Crystal adjustment output. Adjustment is made when the microcomputer is reset. Half the crystal output (32.768 kHz) is given out with jumper provided.	O
34 35 36 37	KEY INPUT 4 KEY INPUT 3 KEY INPUT 2 KEY INPUT 1	4 x 13 matrix is formed by Pin Nos. 41 thru 53 (S1 thru S2). Jumper input or key input is made.	I I
38	Vp	−30V to be connected	

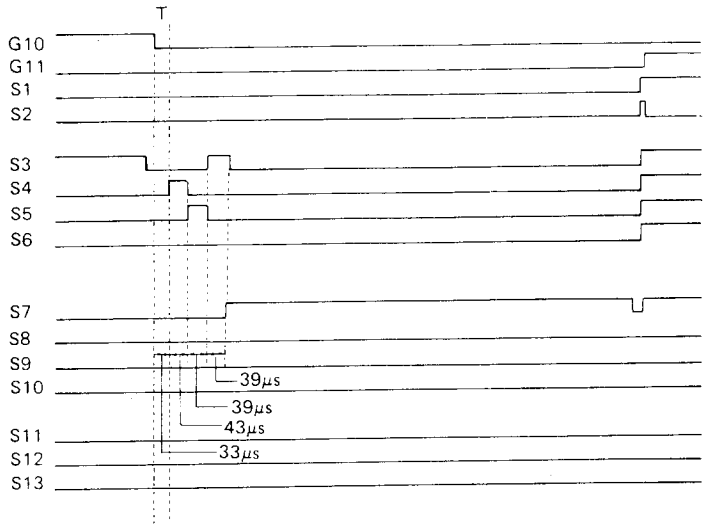


Figure 4-4.

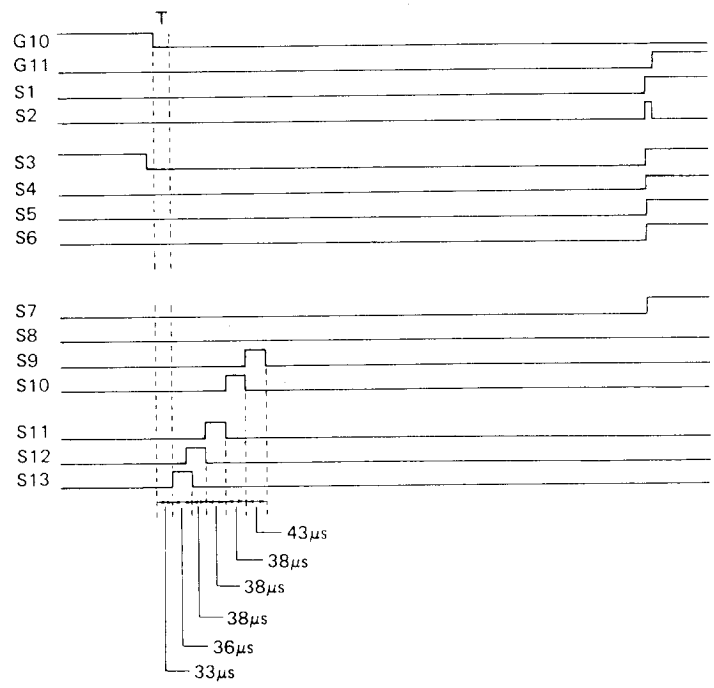
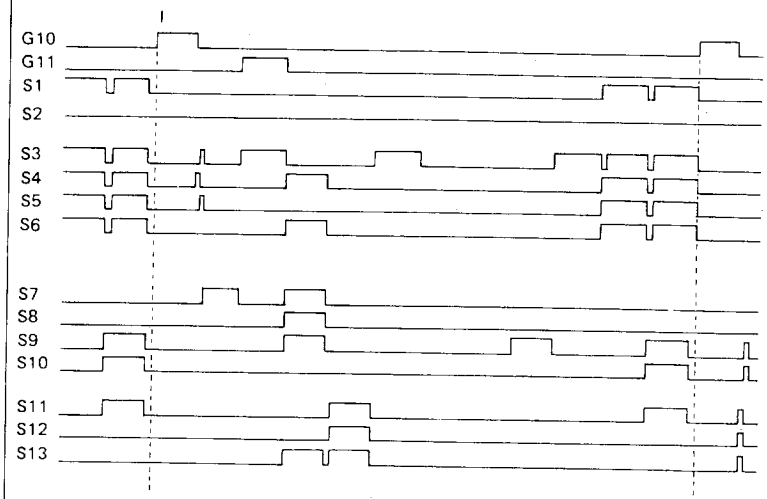
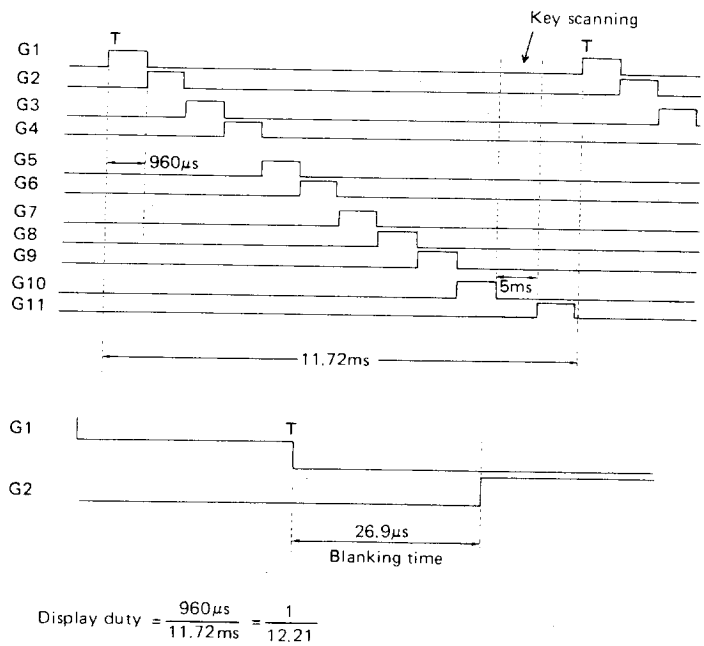
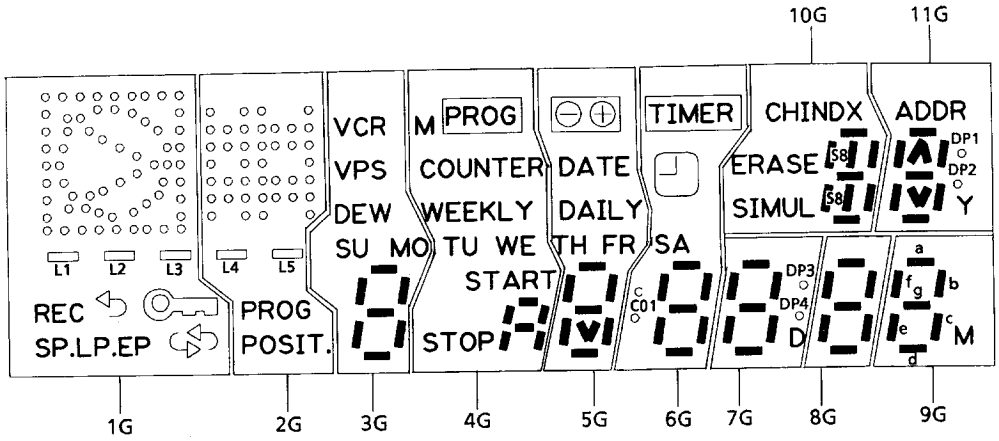


Figure 4-5.

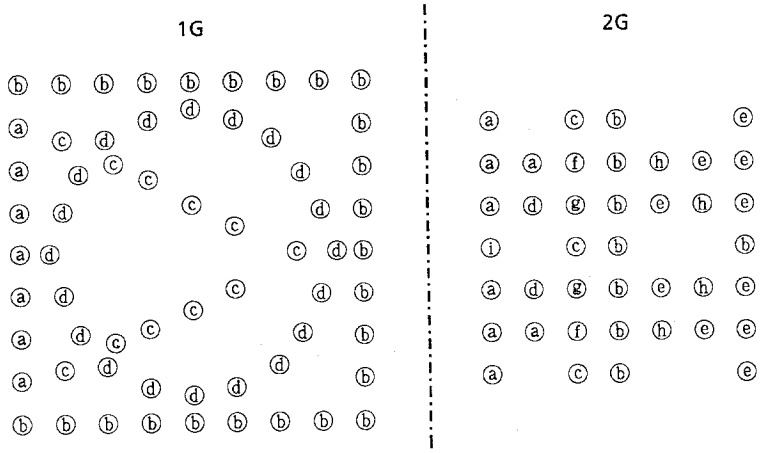
Pin No.	Name	Description	I/O (Type)
39	PAY (H)	Output at "H" while the PAY position is selected.	O (P-CH)
40	NC		
41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64	S8 S1 S2 S6 S7 S3 S5 S4 S9 S10 S11 S12 S13 G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11	Output terminals for fluorescent display tube drive segment signal and key scan strobe signal. (Segment signal) Segment signal output is timed with digit signal output at Pins 54 thru 64.  Figure 4-6. Output terminals for digit signals to drive the fluorescent display tube.  $\text{Display duty} = \frac{960\mu s}{11.72ms} = \frac{1}{12.21}$ Figure 4-7.	O (P-CH) High withstand voltage O (P-CH) High withstand voltage

4-2. DIGITRON DISPLAY

GRID ASSIGNMENT



SEGMENT DESIGNATION



ANODE CONNECTION

	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
S1	a	a	a	a	a	a	a		a	f	EP
S2	b	b	b	b	b	b	b		b	d	LP
S3	c	c	c	c	c	c	c		c	c	d
S4	d	d	d	d	d	d	d	STOP	d	h	a
S5	e	e	e	e	e	e	e	START	e	g	c
S6	f	f	f	f	f	f	f	TU	f	a	SP
S7	g	g	g	g	g	g	g	WE	g	i	b
S8	∧	I I	M	—	D	col 1	TH	WEEKLY	MO	b	□ (L1)
S9	∨	SIMUL	—	—	DP.3	SA	FR	COUNTER	SU	e	□ (L2)
S10	DP.2	ERASE	—	—	DP.4	⌟	DAILY	M	DEW	POSIT.	↺ ↻
S11	DP.1	CH	—	—	—	▭	DATE	—	VPS	PROG	⊶
S12	Y	INDEX	—	—	—	TIMER	⊖ ⊕	PROG	VCR	□ (L5)	REC ↻
S13	ADDR	—	—	—	—	—	∨	—	—	□ (L4)	□ (L3)

4-3. DATA TRANSFER FROM TIMER TO SYSTEM CONTROLLER

(1) Format of Data Transferred from Timer to SYSCON

1) 5-byte data are transferred in one transfer sequence.
2) T0 and T1 bytes, which are each composed of 8-bit data, are designated as remote control data.
3) Remote control data, which are described in the table mentioned late are determined by control signals from infrared remote control and timer.
4) T0 and T1 bytes always have the same data.
5) System controller validates the contents of remote control data by judging that the data of T0 byte conform to those of T1 byte.
6) T2, T3 and T4 bytes, which are each composed of 8-bit data, are designated as timer status data.
7) Timer status data, composed of 8-bit flag and described in the format mentioned later, express the state of timer, etc.
8) System controller, when receiving the same timer status data twice consecutively, validates their contents.

(1) T0/T1 BYTE DATA FORMAT

T0, T1 BYTE DATA FORMAT

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	CH9	CH10	NOTE 1	NOTE 2	LOCK KEY	SRT START	SRT LENGTH
1	REPEAT	CH UP	CH DOWN	TV / VIDEO	VOL UP	VOL DOWN	POWER	AUDIO MUTE	AUDIO MODE	TIMER	MULT1 STROBO	CH CALL	OSD	PROG	SET	REC SPEED
2	PROG CLEAR	FF	PLAY	REW	F.ADV	PAUSE	REV F.ADV	STOP	REC	SLOW	SEARCH	POWER OFF	CLOCK SET	FWD	REV	SLOW UP
3	SLOW DOWN	DS PB	REV PB	EJECT	SOUCE CHANGE	STROBO	TV STILL	COLOR ART	PAINTING	TIMER OFF	P in P	SHIFT	MENO	DISCO	CH MULT1	GOTO
4	NOP										TRACKING MAX	TRACKING MIN	TEST REC	Timer TEST1	Timer TEST2	Timer TEST3
5																
6		LOW SPEED FF	AUTO VSF	LOW SPEED REW				TIMER STOP	TIMER REC	TIMER INT			BOOMERANG REW	STOP		
7		AUTO FF	AUTO PB	AUTO REW	COMPEN-SATION REW			AUTO STOP								
8	NOP			COUNTER O BACK	COUNTER RESET	TRACKING +	TRACKING −	CH MEMORY	EDIT IN	EDIT OUT			COUNTER CLOCK	MOD OSD	REMAIN	CONFIRM OPERATION
9							TRACKING CENTER									
A	J/S + SLOW 1	J/S -SLOW 1	J/S + SLOW 2	J/S -SLOW 2	J/S + PLAY	J/S -PLAY	J/S + SERCH 1	J/S -SERCH 1	J/S + SERCH 2	J/S -SERCH 2	J/S + SERCH 3	J/S -SERCH 3	J/S + FA	J/S -FA		
B																
C	NOP															
D																
E																
F																

NOTE 1) NTSC : CH11, PAL : −/+
NOTE 2) NTSC : CH12

● 2 byte data format

T_{27}	T_{26}	T_{25}	T_{24}	T_{23}	T_{22}	T_{21}	T_{20}

T2 byte

1) T2 byte is timer status data.

T_{20}: LP mode (1/3 x) - L (EP-L)
T_{21}: LP mode (1/2 x) - L (LP-L)
T_{22}: Timer mode (TMOD)
T_{23}: Buzzer 1 (Short sound)
T_{24}: Buzzer 2 (Long sound)
T_{25}: Interruption mode
T_{26}: Scan enable (SCANE)
T_{27}: AUX mode (AUX)

EP-L	LP-L	Mode
0	1	LP mode (1/3 x)
1	0	LP mode (1/2 x)
1	1	Standard mode
0	0	SP fixed mode

● 3 byte data format

T_{37}	T_{36}	T_{35}	T_{34}	T_{33}	T_{32}	T_{31}	T_{30}

T3 byte

2) T3 byte is timer status data.

T_{30}: Index mode (INDEX-MODE)
T_{31}: Electronic lock (E-LOCK)
T_{32}: Introduction enable (INTRO-enable)
T_{33}: Mute request (MUTE-REQUEST)
T_{34}: Last CH flag (last-CH)
T_{35}: CH selection flag (UNDER-TUNING)
T_{36}: Full auto (FULL-AUTO)
T_{37}: Index bit (INDEX-BIT)

● 4 byte data format

T_{47}	T_{46}	T_{45}	T_{44}	T_{43}	T_{42}	T_{41}	T_{40}

T4 byte

3) T4 byte is timer status data.

T_{40}: Door panel flag
T_{41}: MOD OSD
T_{42}: (Spare) → Counter reset
T_{43}: (Spare)
T_{44}: (Spare)
T_{45}: (Spare)
T_{46}: (Spare)
T_{47}: ATR SW (AUTO TRAKING SW)

5. TIMER CIRCUIT RH-iX0589GEZZ (VC-A10/A30/A35/A40/A45/A50 SERIES, VC-A60S, G, Y, H)

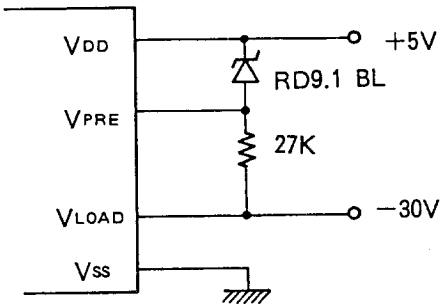
5-1. PIN ASSIGNMENT AND FUNCTIONAL DESCRIPTION OF EACH PIN

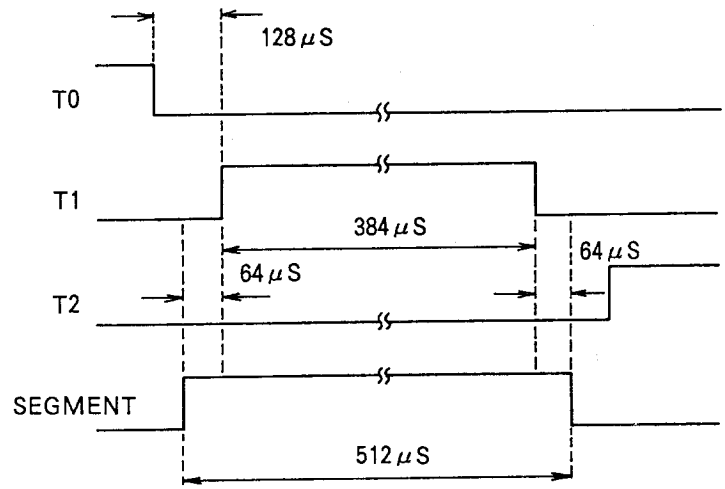
(1) Pin Assignment

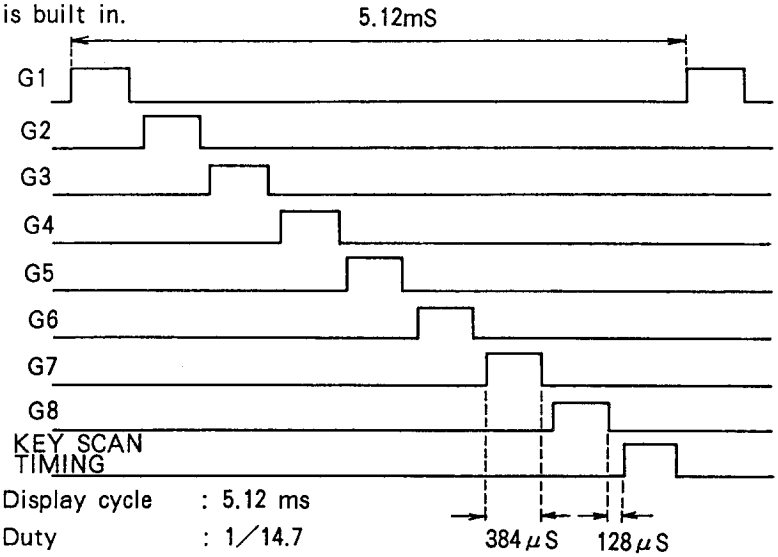
Terminal Name	No.	Name		Name	No.	Terminal Name
S4	1	S3		Vdd	64	+5V
S3	2	S2		S4	63	S5
S2	3	S1		S5	62	S6
S1	4	S0		S6	61	S7
AC PULSE	5	INT4		S7	60	S8
SYSCON TIMER CLK	6	$\overline{SCK}$		S8	59	S9
TIMER SERIAL DATA	7	S0		S9	58	S10
SYSCON SERIAL DATA	8	S1		VPRE	57	−4V
R/C PULSE	9	INTO		VLOAD	56	−30V
SYSCON RDY-L	10	P11		S10	55	S11
CTL PULSE (1/25)	11	INT2		S11	54	S12
GND	12	P13		S12	53	S13
B0	13	P20		S13	52	S14
B1	14	P21	RH-iX0589GEZZ	S14	51	S15
AFT-MUTE	15	P22		S15	50	S16
TUNER P-CON	16	BUZ		T9	49	NC
STEREO-L	17	P30		T8	48	G1
BILINGUAL-L	18	P31		T7	47	G2
STEREO MUTE-H	19	P32		T6	46	G3
E²PROM D I/O	20	P33		T5	45	G4
SCL	21	P60		T4	44	G5
SDA	22	P61		T3	43	G6
AUDIO OUTPUT CTL	23	P62		T2	42	G7
NORMAL-L	24	P63		T1	41	G8
KEY 1	25	P40		T0	40	NC
KEY 2	26	P41		$\overline{RESET}$	39	$\overline{RESET}$
KEY 3	27	P42		P53	38	E²PROM CLK
KEY 4	28	P43		P52	37	E²PROM CS-L
VT	29	PPO		P51	36	VIDEO-TUNER-L
4 MHz	30	X1		P50	35	AUDIO-TUNER-H
4 MHz	31	X2		XT2	34	32.768KHz
GND	32	VSS		XT1	33	32.768KHz

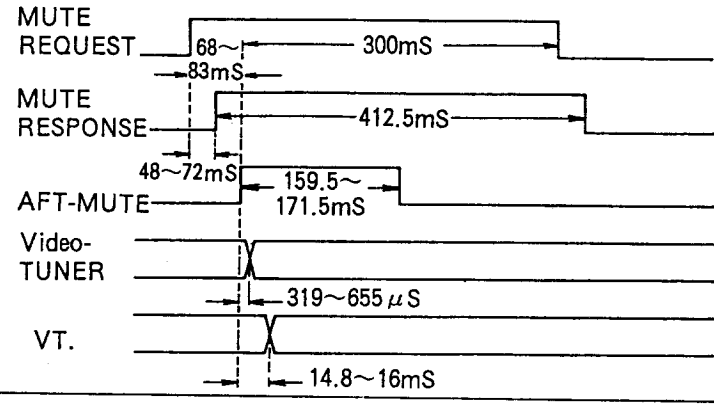
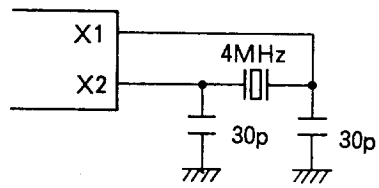
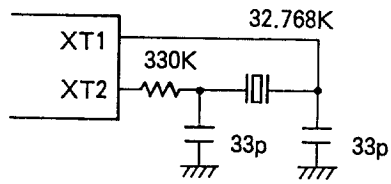
(2) Functional Description of Each Pin

No.	Name	Pin	Description	I/O
64	+5V	V_{DD}	Connected to V_{DD} (+5V).	
32	GND	V_{SS}	Connected to GND (0V).	
56 57	−30V −4V	V_{LOAD} V_{PRE}	Connected to −30V. Connected to −4V.	
4 3 2 1 63 62 61 60 59 58 55 54 53 52 51 50	S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16	S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15	Outputs the segment signals to drive the fluorescent display tube. P-ch is open and a pull-down resistor is built in.	O





No.	Name	Pin	Description	I/O
48 47 46 45 44 43 42 41 40	G1 G2 G3 G4 G5 G6 G7 G8 NC	T8 T7 T6 T5 T4 T3 T2 T1 T0	Outputs the digit signals to drive the fluorescent display tube. P-ch is open and a pull-down resistor is built in.  Display cycle : 5.12 ms Duty : 1/14.7 Digit cut width : 128 μs	O
5	AC PULSE	INT4	Inputs AC pulses to detect power failure. Duty is 25% ~ 75%. If there is no leading and trailing edges of AC pulse for 35 ms, the microcomputer judges as power failure and it goes in power failure mode.	I
6	SYSCON TIMER CLK	$\overline{SCK}$	Used for serial data transfer with system controller (SYSCON). Connected to CLK pin of SYSCON.	O
7	TIMER SERIAL DATA	SO	Used for serial data transfer with SYSCON. Connected to TIMER SERIAL DATA pin of SYSCON.	O
8	SYSCON SERIAL DATA	SI	Used for serial data transfer with SYSCON. Connected to SYSCON SERIAL DATA pin of SYSCON.	I
10	SYSCON READY-L	INT1	Used for serial data transfer with SYSCON. Connected to SYSCON SERIAL DATA pin of SYSCON.	I
9	R/C PULSE	INT0	Inputs pulses from optical remote controller.	I
11	CTL PULSE (1/25)	INT2	Signal to control the real time counter. With P-CON bit=1 and CASSETTE IN bit-1, With the leading and trailing edges of CTL pulse are input, the internal counter counts up 0.5 sec if the counter reverse bit is 0, or the counter counts down 0.5 sec if that bit is 1. Counter reverse bit ····· This is SYSCON serial data`(S34) and it implies forward or reverse of reel head.	I

<table>
<tr><th>No.</th><th>Name</th><th>Pin</th><th>Description</th><th>I/O</th></tr>
<tr><td>13
14</td><td>B0
B1</td><td>P20
P21</td><td>Outputs signal to change over the band.
<table>
<tr><th></th><th>VHF-L</th><th>VHF-H</th><th>UHF</th></tr>
<tr><td>B0</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>B1</td><td>L</td><td>L</td><td>H</td></tr>
</table></td><td>O
O</td></tr>
<tr><td>15</td><td>AFT-MUTE</td><td>P22</td><td>Outputs AFT MUTE signal.

</td><td>O</td></tr>
<tr><td>25
26
27
28</td><td>KEY 1
KEY 2
KEY 3
KEY 4</td><td>P40
P41
P42
P43</td><td>Making up a 4x10 matrix, they input jumper and key signals.
A pull-down resistor must be connected externally.</td><td>I</td></tr>
<tr><td>29</td><td>VT</td><td>PP0</td><td>Outputs the pulse-width modulated wave according to the tuning data of 14 bits.</td><td>O</td></tr>
<tr><td>30
31</td><td>MAIN
SYSTEM
CLOCK</td><td>X1
X2</td><td>The MAIN SYSTEM CLOCK can be got by the recommended circuit as shown below.

</td><td>I
O</td></tr>
<tr><td>33
34</td><td>SUB SYSTEM
CLOCK</td><td>XT1
XT2</td><td>The SUB SYSTEM CLOCK can be got by the recommended circuit as shown below.

</td><td>I
O</td></tr>
<tr><td>35
36</td><td>AUDIO-TUNER
VIDEO-TUNER</td><td>P50
P51</td><td>Outputs signal to change over input mode.
<table>
<tr><th></th><th>TUNER mode</th><th>SIMUL mode</th><th>AUX mode</th></tr>
<tr><td>VIDEO-TUNER</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>AUDIO-TUNER</td><td>H</td><td>L</td><td>L</td></tr>
</table></td><td>O
O</td></tr>
</table>

<table>
<tr><th>No.</th><th>Name</th><th>Pin</th><th>Description</th><th>I/O</th></tr>
<tr><td>20</td><td>E²PROM
DATA I/O</td><td>P33</td><td>Connectd to D1 and D0 (via resistor for D0) pins of E²PROM.</td><td>I/O</td></tr>
<tr><td>37</td><td>E²PROM CS-L</td><td>P52</td><td>Connected to CS pin of E²PROM.</td><td>O</td></tr>
<tr><td>38</td><td>E²PROM CLK</td><td>P53</td><td>Connected to CLK pin of E²PROM.</td><td>O</td></tr>
<tr><td>39</td><td>RESET</td><td>RESET</td><td>The microcomputer is reset by RESET = "L"
This pin must be on "L" level (0V – 0.2V) for more than 10 ms.</td><td>I</td></tr>
<tr><td>15</td><td>TUNER P-CON</td><td>BUZ</td><td>Signal to control the tuner power in order to receive VPS code even when power is off in TIMER STAND-BY mode.
To be held at "H" when VPS timer value is being detected or when recording by VPS timer is being executed.
* Functions as PAY-"H" output terminal when VPS jumper is not provided.

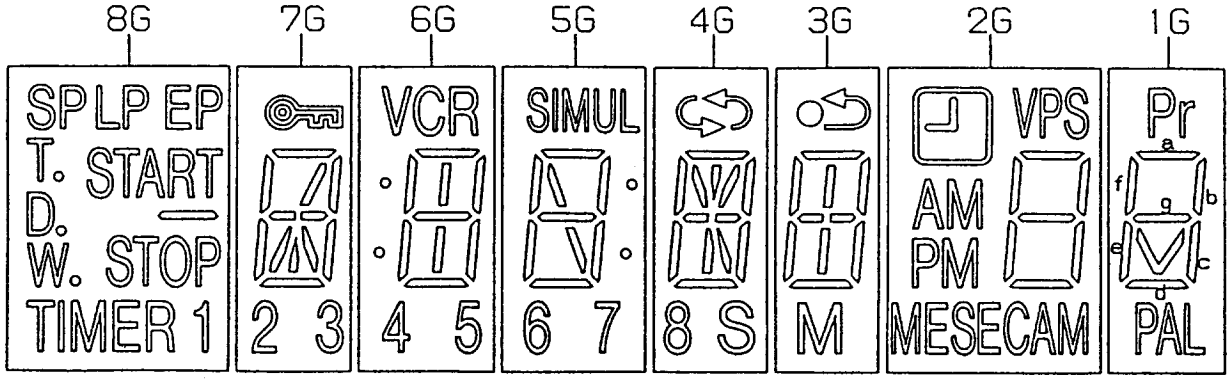
PAY-CH
<table><tr><th></th><th>PAY-CH</th></tr><tr><td>39-position AUS jumper provided</td><td>29~38</td></tr><tr><td>39-position AUS jumper not provided</td><td>30~39</td></tr><tr><td>50-position AUS jumper provided</td><td>40~49</td></tr><tr><td>50-position AUS jumper not provided</td><td>41~50</td></tr></table></td><td>O</td></tr>
<tr><td>21</td><td>SCL</td><td>P60</td><td rowspan="2">Terminal to control the I²C bus used for serial communication with VPS decoder.
Also used for communication with sound multiplex IC.</td><td>I/O</td></tr>
<tr><td>22</td><td>SDA</td><td>P61</td><td>I/O</td></tr>
<tr><td>17</td><td>STEREO-L</td><td>P30</td><td rowspan="2">Terminal to control "STEREO" /"BILINGUAL" indicator ON/OFF; effective only when sound multiplex port jumper is provided.
<table><tr><th></th><th>STEREO indicator</th><th>BILINGUAL indicator</th></tr><tr><td>STEREO-L input ; "L"</td><td>ON</td><td>Don't care</td></tr><tr><td>STEREO-L input ; "H"</td><td>OFF</td><td></td></tr><tr><td>BILINGUAL-L input ; "L"</td><td>Don't care</td><td>ON</td></tr><tr><td>BILINGUAL-L input ; "H"</td><td></td><td>OFF</td></tr></table></td><td>I</td></tr>
<tr><td>18</td><td>BILINGUAL</td><td>P31</td><td>I</td></tr>
</table>

<table>
<tr><th>No.</th><th>Name</th><th>Pin</th><th>Description</th><th>I/O</th></tr>
<tr><td>19</td><td>STEREO-MUTE
"H"</td><td>P32</td><td>Terminal to control the muting circuit
<table><tr><th></th><th>STEREO MUTE-H</th><th>AFT-MUTE</th><th>STEREO/BILINGUAL indicator</th></tr><tr><td>PRESET</td><td>Decided by SYNC (*1)</td><td>H</td><td></td></tr><tr><td>AUX</td><td>H</td><td>L</td><td>OFF</td></tr><tr><td>SIMUL</td><td>Decided by SYNC (*1)</td><td>L</td><td>OFF</td></tr><tr><td>PLAYBACK</td><td>H</td><td>L</td><td>OFF</td></tr><tr><td>PCON = L</td><td>L</td><td>L</td><td>OFF</td></tr></table>※<table><tr><td>SYNC provided</td><td>L</td></tr><tr><td>SYNC not provided</td><td>H</td></tr></table></td><td>O</td></tr>
<tr><td>24</td><td>NORMAL-L</td><td>P63</td><td>Terminal to control L/R indicator ON/OFF : L or R indicator, or both L and R indicators light up and go out by "H" input and "L" input, respectively. "L" output takes precedence when the mode is turned into NORMAL by the timer.
<table><tr><th>P-CON</th><th>MODE</th><th>AUDIO OUTPUT CTL</th><th>"L" seg</th><th>"R" seg</th><th>NORMAL (L) terminal</th></tr><tr><td rowspan="4">[H]</td><td>STEREO (Main/Sub)</td><td>ON</td><td>ON</td><td>ON</td><td>Input mode (*1)</td></tr><tr><td>Left (Main)</td><td>ON</td><td>ON</td><td>OFF</td><td>Input mode (*1)</td></tr><tr><td>Right (Sub)</td><td>OFF</td><td>OFF</td><td>ON</td><td>Input mode (*1)</td></tr><tr><td>Forced NORMAL</td><td>OFF</td><td>OFF</td><td>OFF</td><td>(L) output mode</td></tr><tr><td>[L]</td><td>———</td><td>OFF</td><td>OFF</td><td>OFF</td><td>Previous mode retained</td></tr></table>*1 : In input mode, L and R indicators go out when NORMAL (L) terminal input is at "L".</td><td>I/O</td></tr>
<tr><td>12</td><td>GND</td><td>P13</td><td>To be connected with ground. Usually not used.</td><td>—</td></tr>
<tr><td>49</td><td>NC</td><td>P9</td><td>Used for NC mode.</td><td>—</td></tr>
</table>

5-2. DIGITRON DISPLAY

The following shows the grid assignment and anode connection of the digitron display.

GRID ASSIGNMENT



ANODE CONNECTION

	8G	7G	6G	5G	4G	3G	2G	1G
S1	SP	a	a	a	a	a	a	a
S2	T.	b	b	b	b	b	b	b
S3	STOP	c	c	c	c	c	c	c
S4	–	d	d	d	d	d	d	d
S5	W.	e	e	e	e	e	e	e
S6	LP	f	f	f	f	f	f	f
S7	D.		g	g			g	g
S8	START			• (上)				–
S9	—						AM	–
S10	1	2					PM	
S11	TIMER	3	4	• (下)		M	MESECAM	PAL
S12	EP		VCR	SIMUL			VPS	Pr
S13	–		5	6	8	–	–	–
S14	–		–	7		–	–	–
S15	–	–	–	–		–	–	–
S16	–	–	–	–	S	–	–	–

5-3. DATA TRANSFER FROM TIMER TO SYSCON

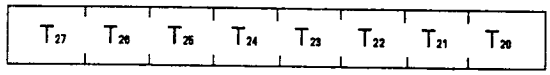
(1) Format of Data Transfer from Timer to SYSCON

i) One-time transfer sequence transfers 5-byte data.
ii) The TO byte and T1 byte comprises respectively 8-bit data, which is remote control (REMOCON) data.
iii) The REMOCON data, as shown in table on the following page, is determined by the control signal from optical REMOCON and timer.
iv) The contents of T0 byte and T1 byte are always same.
v) The SYSCON makes the REMOCON data valid when T0 byte and T1 byte are matched.
vi) The T2 byte, T3 byte and T4 byte comprises respec-tively 8-bit data, which is timer status data.
vii) The timer status consists of 8-bit flags of which format is shown later.
viii) The SYSCON makes the timer status valid when it receives the same timer status twice continuously.

(T0 / T1 Byte Data Format)

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		1	2	3	4	5	6	7	8	9	10	-/--	VPS	LOCK KEY	SRT START	SRT LENGTH
1	REPEAT	CH UP	CH DOWN	TV / VIDEO	VOL UP	VOL DOWN	POWER	AUDIO MUTE	AUDIO MODE	TIMER	MULTI STROBO	CH CALL	OSD	PROG	SET	REC SPEED
2	PROG CLEAR	FF	PLAY	REW	F.ADV	PAUSE	REV F.ADV	STOP	REC	SLOW	SEARCH	POWER OFF	CLOCK SET	FWD	REV	SLOW UP
3	SLOW DOWN	DS PB	REV PB	EJECT	SOUCE CHANGE	STROBO	TV STILL	SEARCH	PAINT ING	TIMER OFF	P in P	SHIFT	MULTI INDEX	DISCO	CH MULTI	GOTO
4	NOP							TEST			TRAC MAX	KING MIN	TEST REC	TIMER TEST1	TIMER TEST2	TIMER TEST3
5																
6		LOW SP EED FF	AUTO VSF	LOW SP EED REW	AUTO VSR			TIMER STOP	TIMER REC	TIMER INT	INSERT STOP		BOOM REW	ERAN STOP		
7		AUTO FF	AUTO PB	AUTO REW	COMP. REW			AUTO STOP	TIMER DATA out	TIMER DATA in		AUTO VISS	MVI REW			
8	NOP	VISS WRITE	VISS ERASE	COUNTER 0 BACK	COUNTER RESET	TRAC +	KING −	CH MEMORY	EDIT IN	EDIT OUT	ADUB	INSERT	COUNTER CLOCK	MODE OSD	REMAIN	OPE. CONFIRM
9			SKIP SEARCH	TITLE	MONITOR	COLOR	TRACKIN CENTER	PRESET	TEXT/ MENU							
A	J/S +SLOW1	J/S −SLOW1	J/S +SLOW2	J/S −SLOW2	J/S +PLAY	J/S −PLAY	J/S +SERCH	J/S −SERCH	J/S +SERCH	J/S −SERCH	J/S +SRCH3	J/S −SERCH	J/S +FA	J/S −FA		
B																
C	NOP															
D																
E																
F																

(2) T2 Byte Data Format



T2 byte

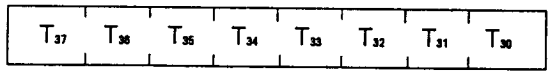
The T2 byte is timer status data.

T_{20} : Triple speed mode - L (EP-L)
T_{21} : Double speed mode - L (LP-L)
T_{22} : Timer mode (TMOD)
T_{23} : Buzzer 1 (short sound: 40ms)
T_{24} : Buzzer 2 (long sound : 1s)
T_{25} : Interrupt (for VPS)
T_{26} : Scan enable
T_{27} : AUX mode

EP-L	LP-L	Mode
0	2	Triple speed
1	0	Double speed
1	1	Standard
0	0	Note 1

Note 1: SP fixed mode

(3) T3 Byte Data Format

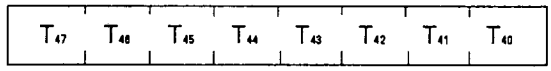


T3 byte

The T3 byte is timer status data.

T_{30} : Index (INDEX-MODE)
T_{31} : Electronic lock (E-LOCK)
T_{32} : Introduction enable (INTRO-E)
T_{33} : Mute request (MUTE-RQU)
T_{34} : Last channel (LAST-CH)
T_{35} : Channel is being tuned (UNDER-TUNING)
T_{36} : Full automatic (FULL-AUTO)
T_{37} : Index detection (INDEX-DETECT)

(4) T4 Byte Data Format



T4 byte

The T4 byte is timer status data.

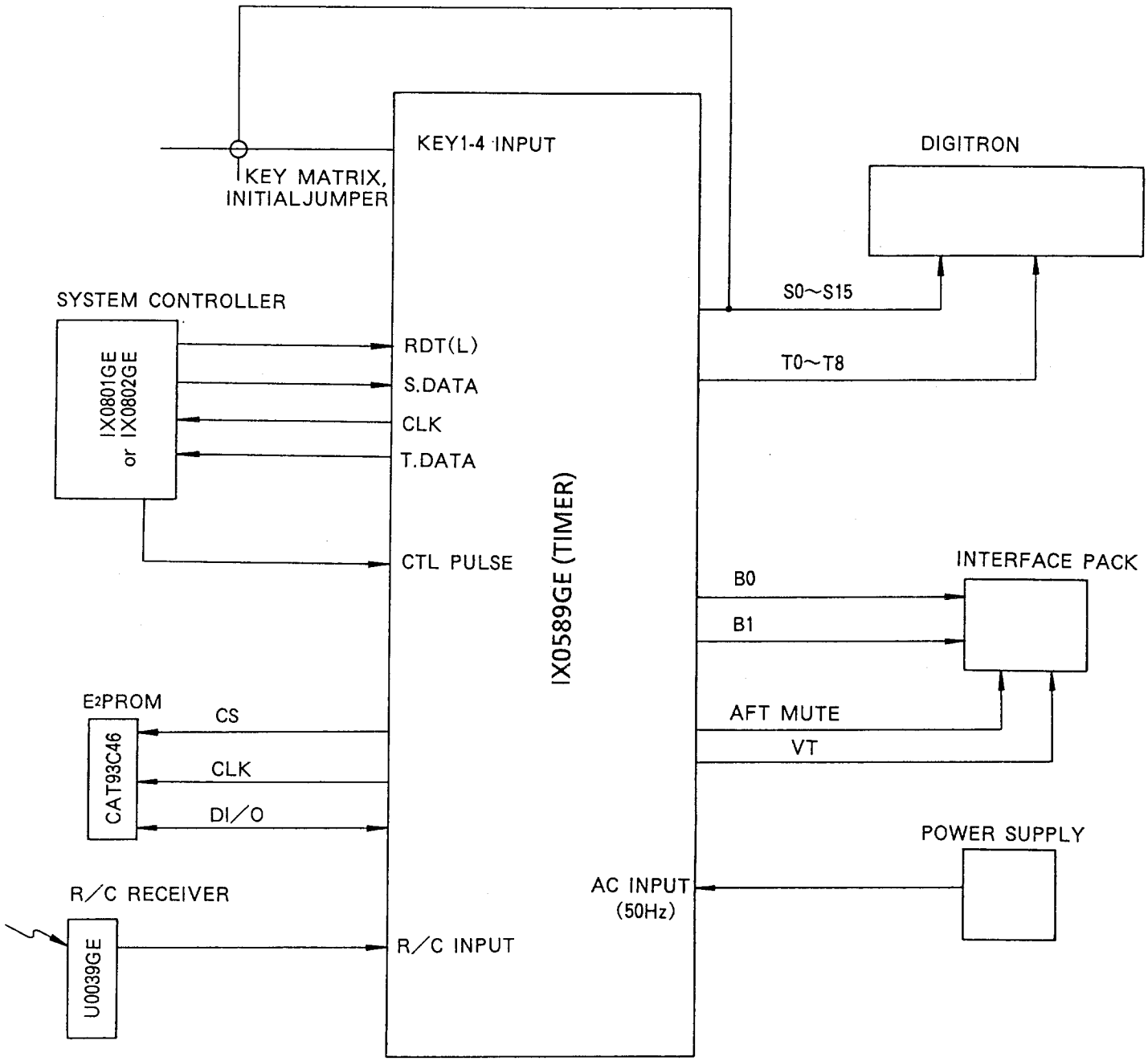
T_{40} : Door panel close (DOOR-CLOSE)
T_{41} : Mode OSD
T_{42} : Counter reset
T_{43} : AUDIO-TUNER
T_{44} : TEXT mode
T_{45} : PAL
T_{46} : MESECAM
T_{47} : ATR

Changeover between TUNER, AUX and SIMUL

	TUNER	AUX	SIMUL	Not used
AUX (T_{27})	0	1	0	1
A-TUNER(T_{43})	1	0	0	1

5-4. BLOCK DIAGRAM AND BASIC CIRCUIT DIAGRAM

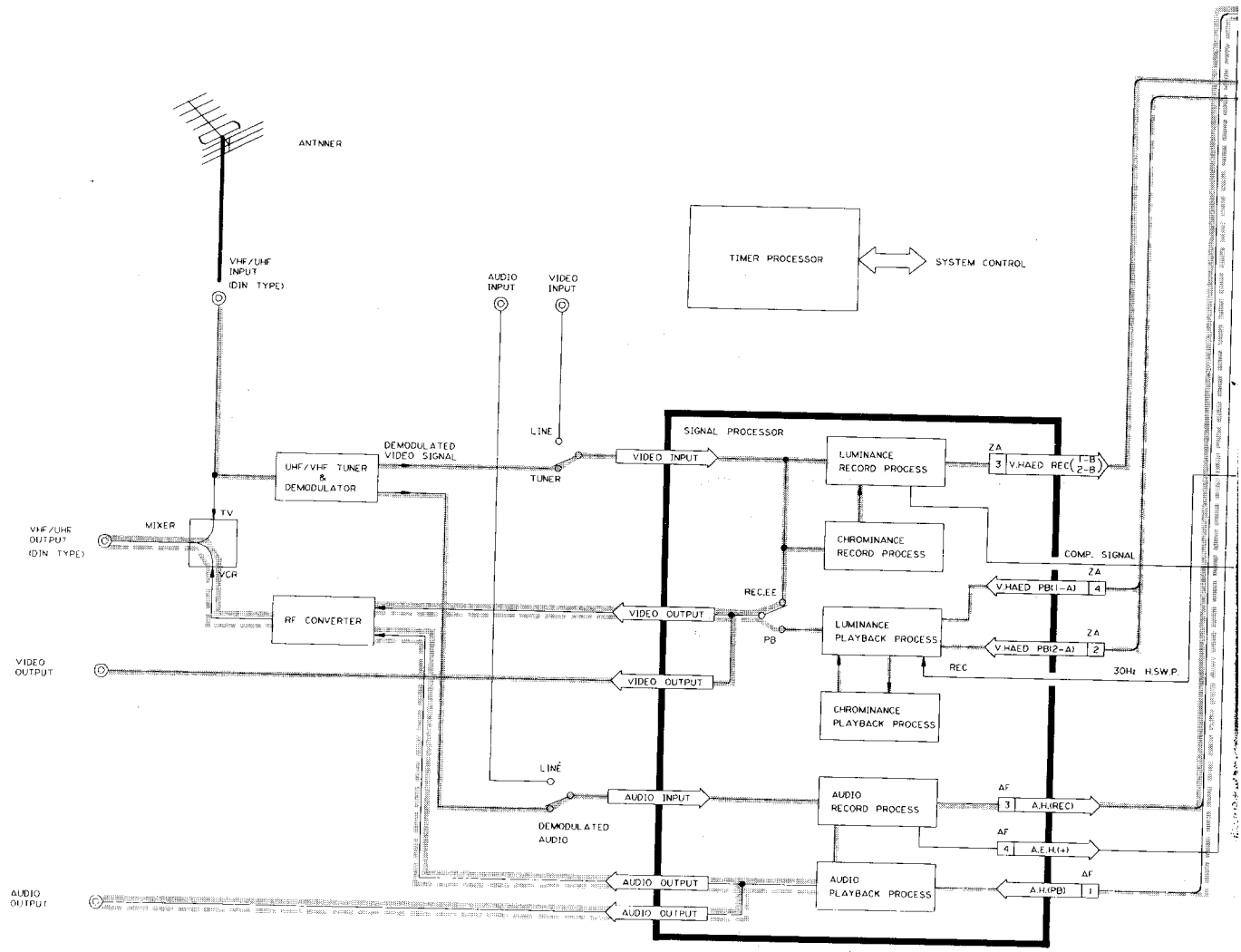
(1) Block Diagram

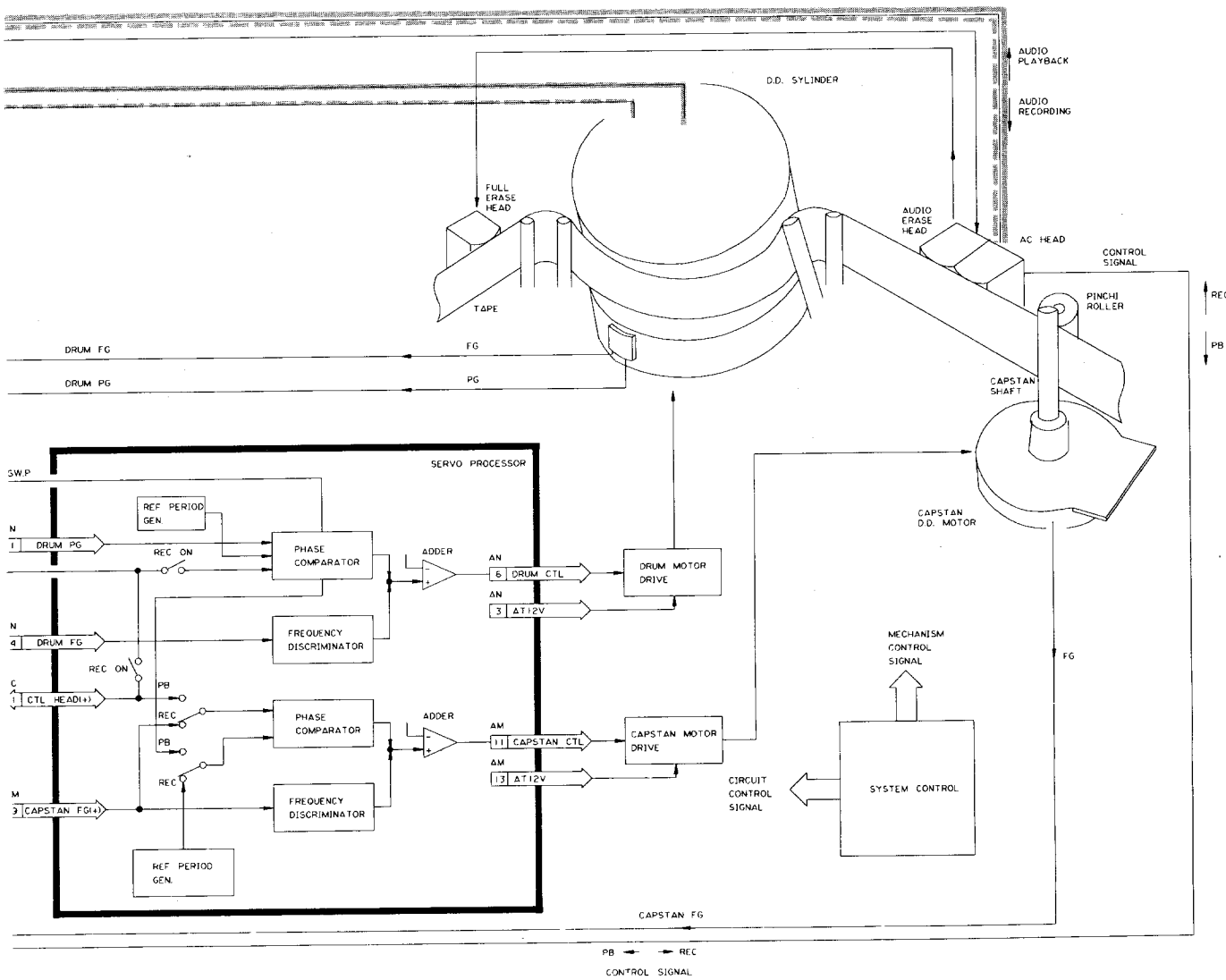


OVERALL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES

SIGNAL PATH REC MODE

SIGNAL PATH PB MODE

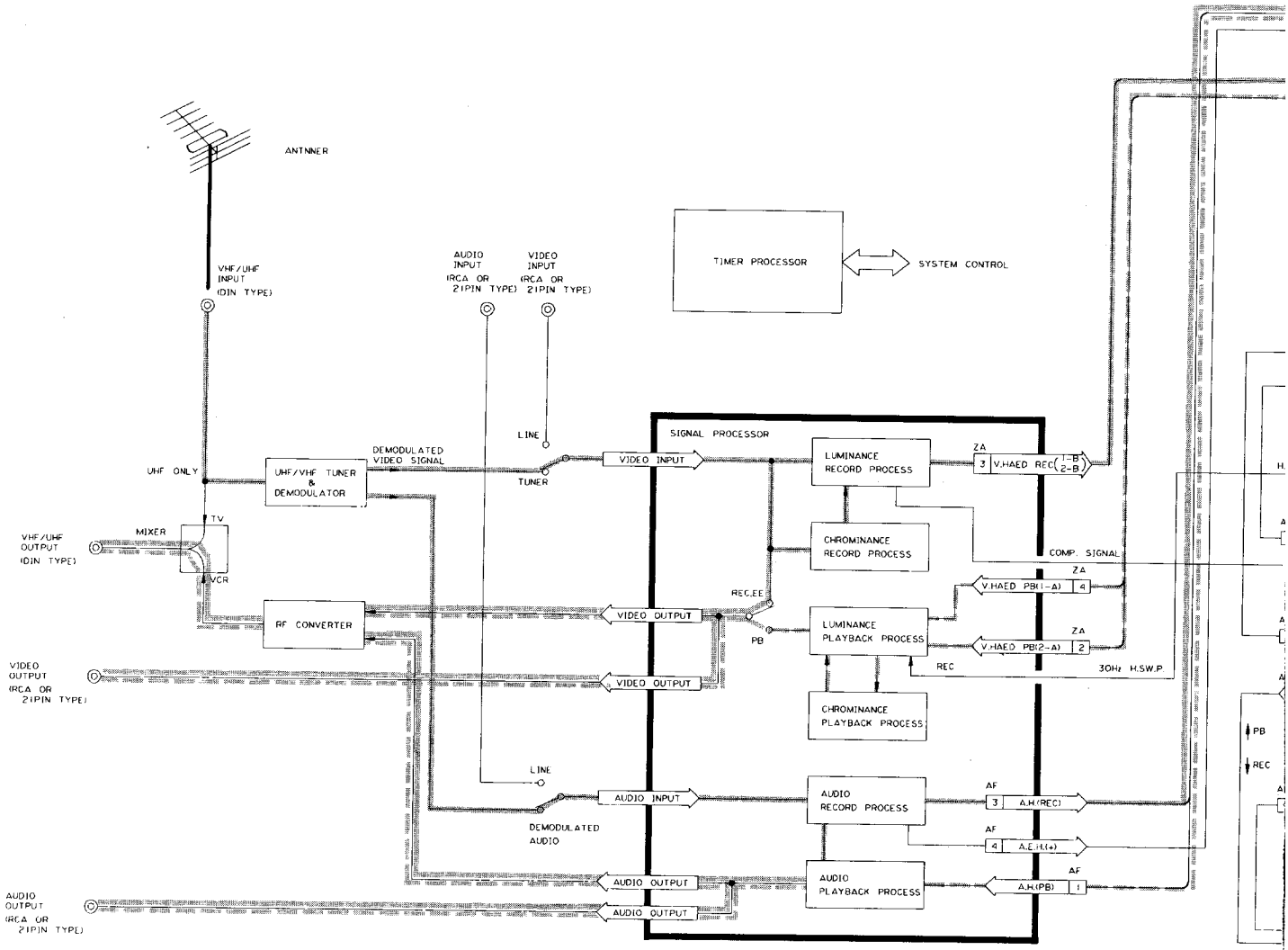


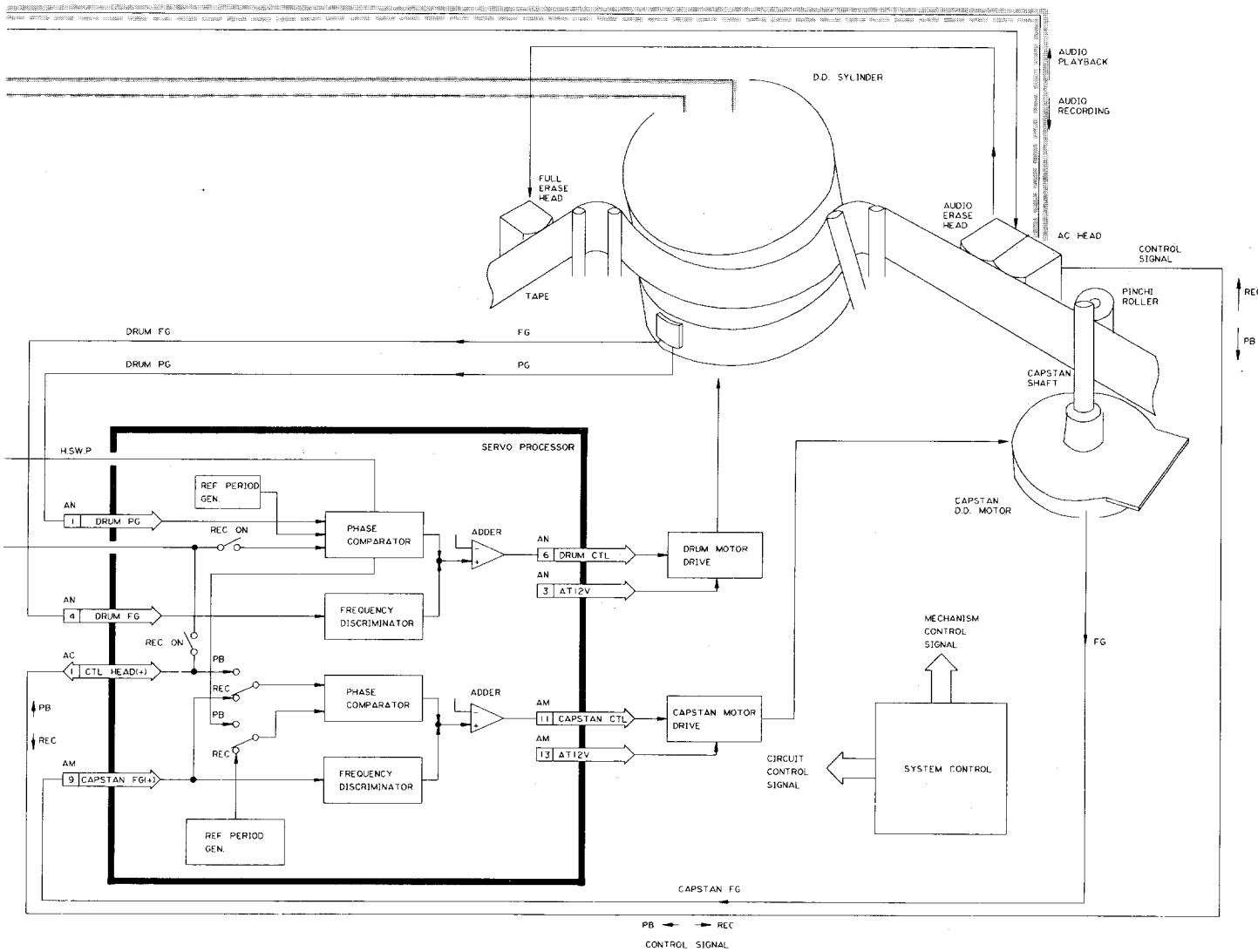

AUDIO PLAYBACK
AUDIO RECORDING
D.D. SYLINDER
FULL ERASE HEAD
AUDIO ERASE HEAD
AC HEAD
CONTROL SIGNAL
TAPE
PINCH ROLLER
REC
PB
DRUM FG
FG
DRUM PG
PG
CAPSTAN SHAFT
SERVO PROCESSOR
SW.P
REF PERIOD GEN.
DRUM PG
REC ON
PHASE COMPARATOR
ADDER
AN
6 DRUM CTL
DRUM MOTOR DRIVE
AN
3 AT12V
FREQUENCY DISCRIMINATOR
DRUM FG
REC ON
CTL HEAD(+)
PB
REC
PB
PHASE COMPARATOR
ADDER
AM
11 CAPSTAN CTL
CAPSTAN MOTOR DRIVE
AM
13 AT12V
REC
CAPSTAN FG(+)
FREQUENCY DISCRIMINATOR
REF PERIOD GEN.
CAPSTAN D.D. MOTOR
MECHANISM CONTROL SIGNAL
FG
CIRCUIT CONTROL SIGNAL
SYSTEM CONTROL
CAPSTAN FG
PB
REC
CONTROL SIGNAL

OVERALL BLOCK DIAGRAM
(FOR 2-HEAD MODELS) : VC-A30/A35/A40/A45 SERIES

SIGNAL PATH REC MODE

SIGNAL PATH PB MODE

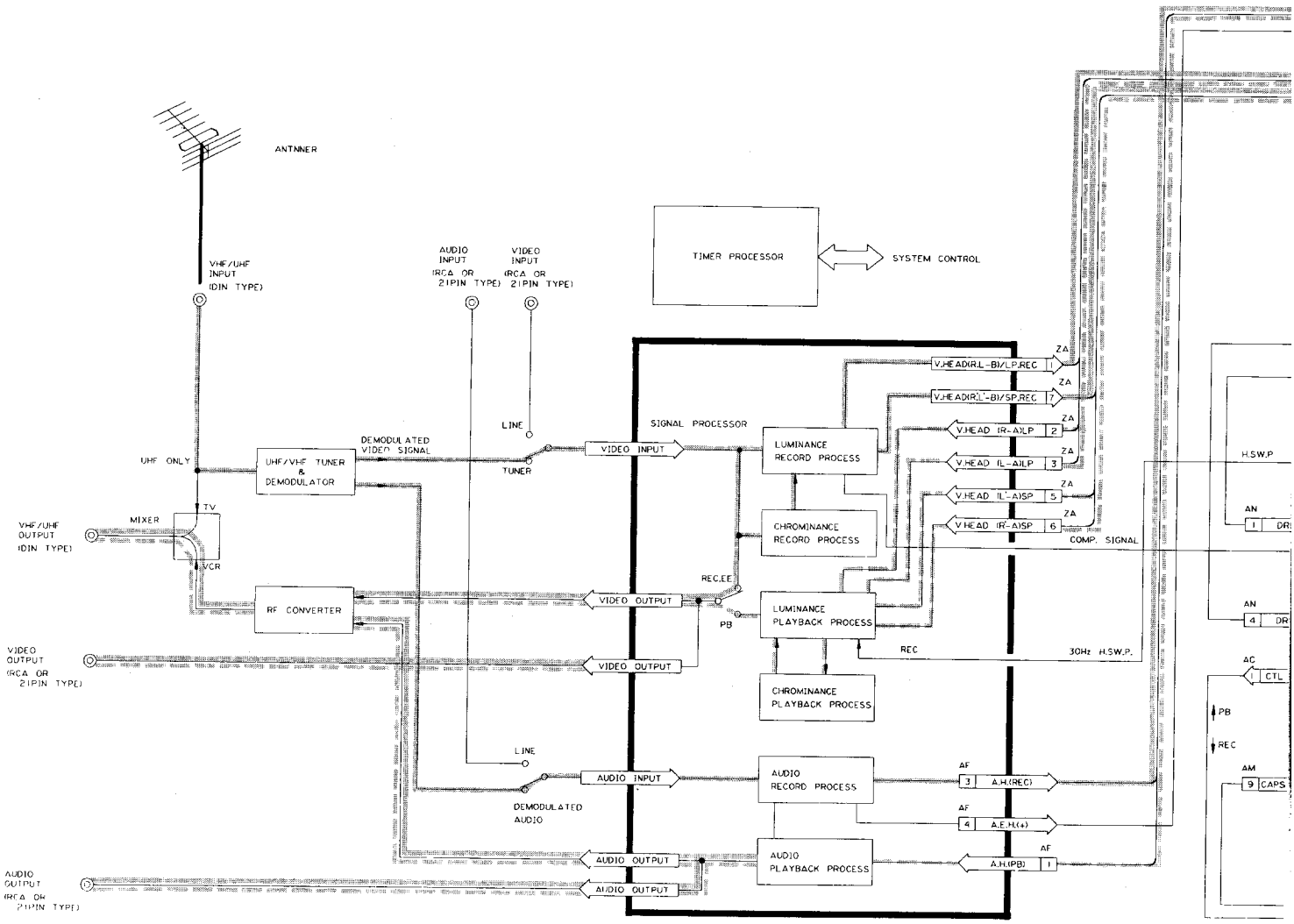


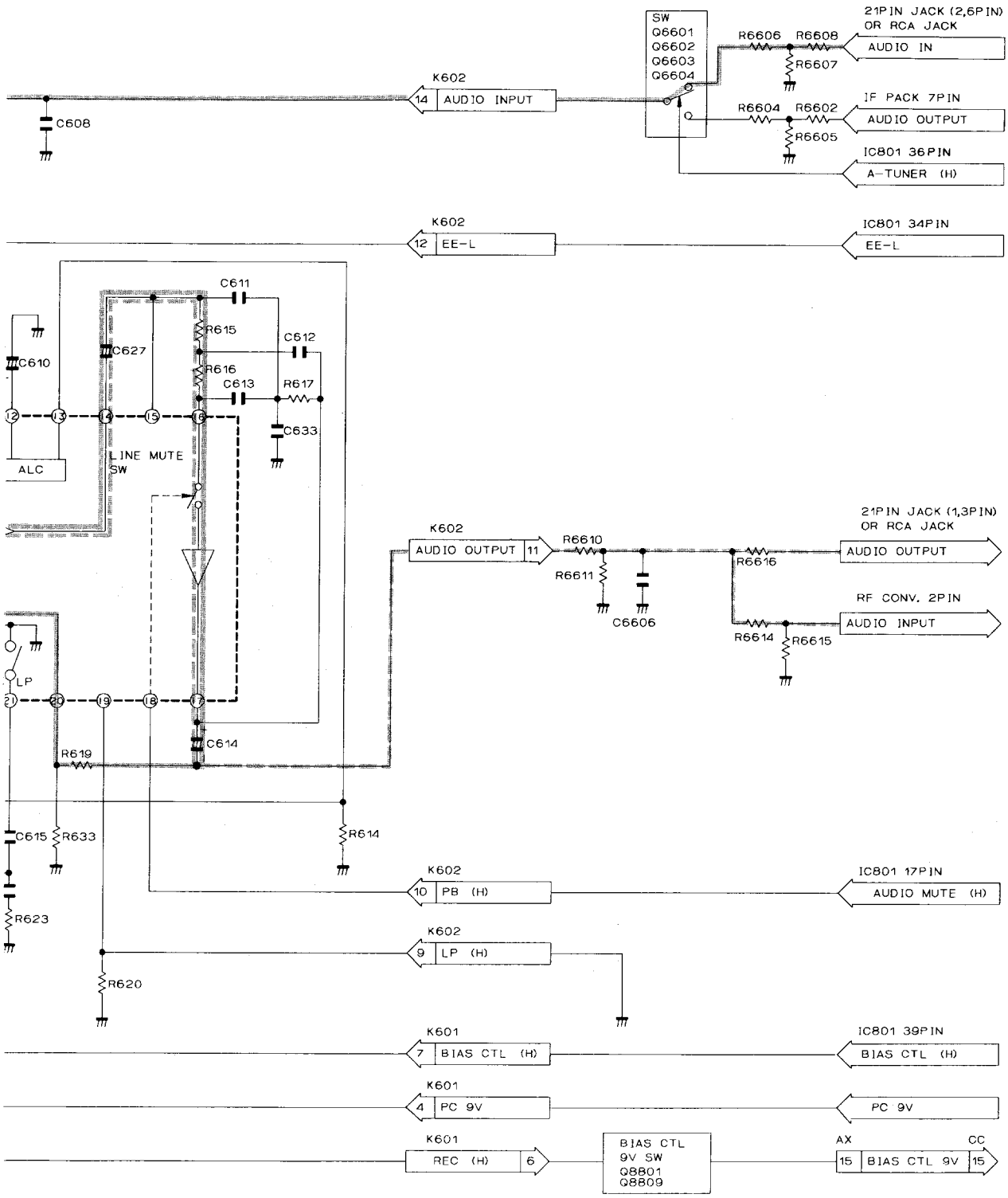

AUDIO PLAYBACK
AUDIO RECORDING
D.D. SYLINDER
FULL ERASE HEAD
AUDIO ERASE HEAD
AC HEAD
CONTROL SIGNAL
REC
PB
PINCHI ROLLER
TAPE
DRUM FG
FG
DRUM PG
PG
CAPSTAN SHAFT
H.SW.P
SERVO PROCESSOR
REF PERIOD GEN.
AN
1 DRUM PG
REC ON
PHASE COMPARATOR
ADDER
AN
6 DRUM CTL
DRUM MOTOR DRIVE
AN
3 AT12V
CAPSTAN D.D. MOTOR
AN
4 DRUM FG
FREQUENCY DISCRIMINATOR
REC ON
AC
1 CTL HEAD(+)
PB
REC
PHASE COMPARATOR
ADDER
AM
11 CAPSTAN CTL
CAPSTAN MOTOR DRIVE
MECHANISM CONTROL SIGNAL
FG
PB
REC
AM
13 AT12V
AM
9 CAPSTAN FG(+)
FREQUENCY DISCRIMINATOR
CIRCUIT CONTROL SIGNAL
SYSTEM CONTROL
REF PERIOD GEN.
CAPSTAN FG
PB
REC
CONTROL SIGNAL

OVERALL BLOCK DIAGRAM (FOR 4-HEAD MODELS) : VC-A50/A60/A61/A62 SERIES

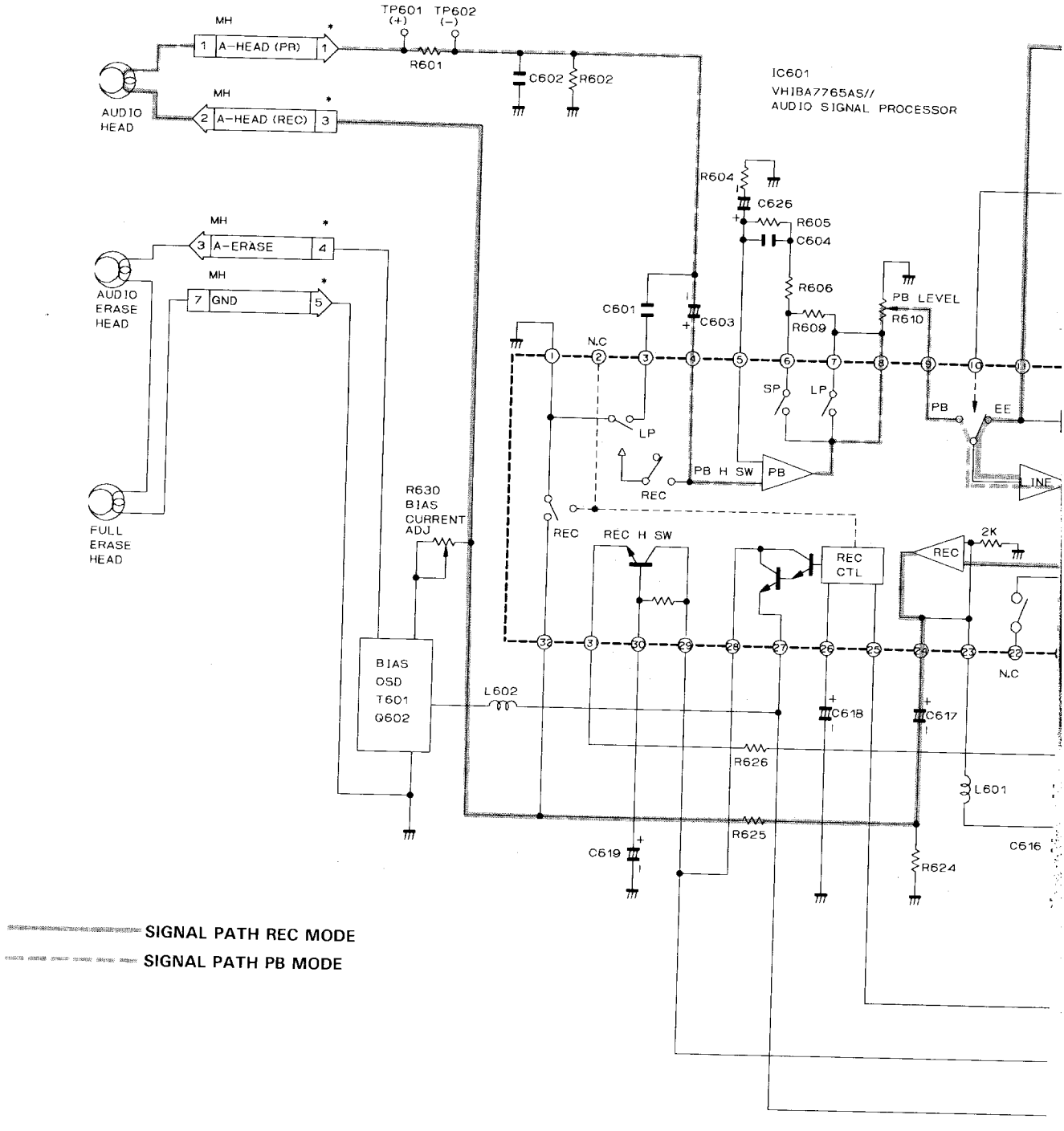
SIGNAL PATH REC MODE

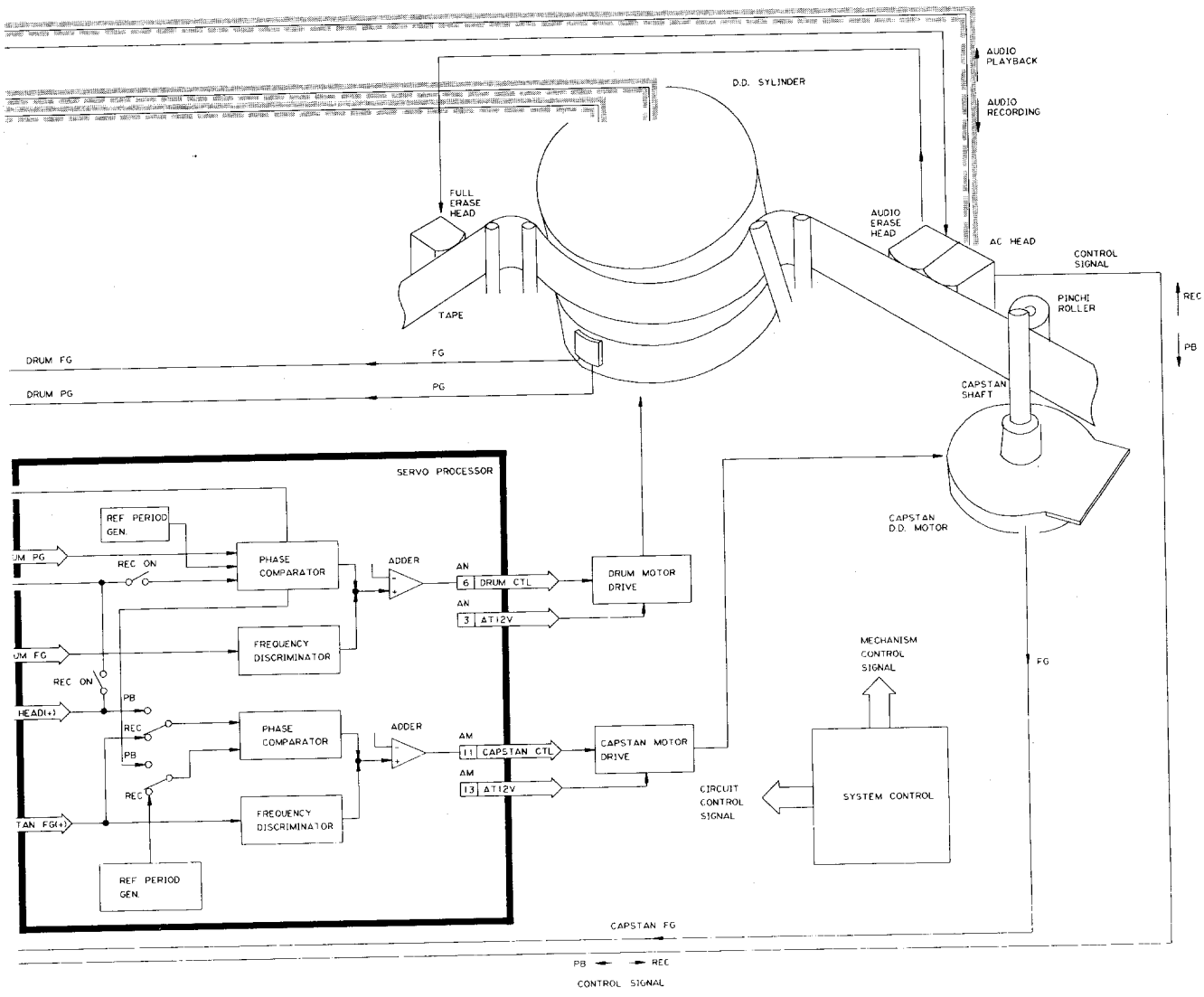
SIGNAL PATH PB MODE



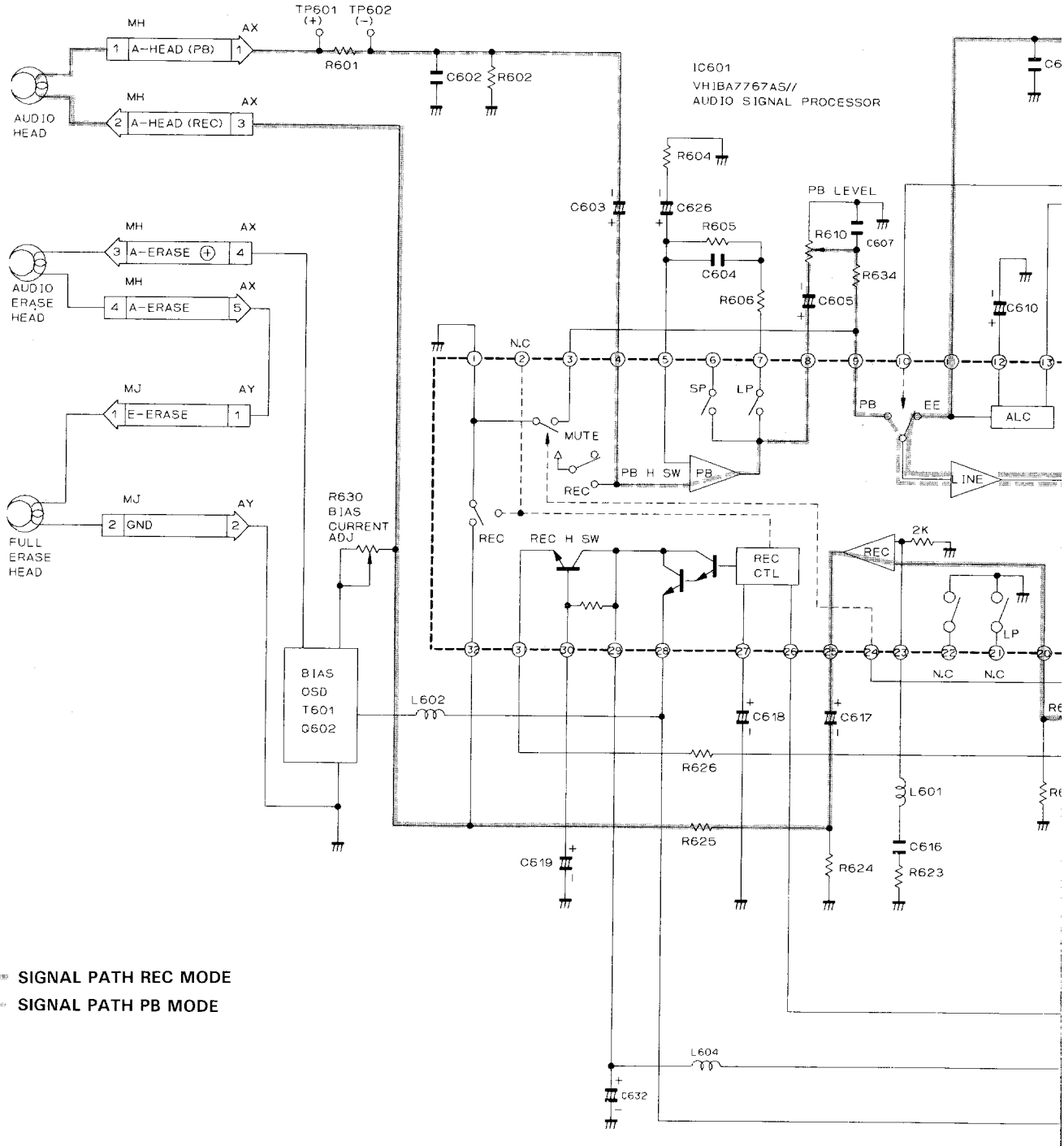

SW
Q6601
Q6602
Q6603
Q6604
21PIN JACK (2,6PIN)
OR RCA JACK
AUDIO IN
R6606
R6608
R6607
IF PACK 7PIN
AUDIO OUTPUT
R6604
R6602
R6605
IC801 36PIN
A-TUNER (H)
K602
14 AUDIO INPUT
C608
K602
12 EE-L
IC801 34PIN
EE-L
C611
R615
C612
C627
C610
R616
C613
R617
C633
ALC
LINE MUTE
SW
21PIN JACK (1,3PIN)
OR RCA JACK
K602
AUDIO OUTPUT 11
R6610
R6611
C6606
R6616
AUDIO OUTPUT
RF CONV. 2PIN
AUDIO INPUT
R6614
R6615
LP
C614
R619
C615
R633
R614
R623
K602
10 PB (H)
IC801 17PIN
AUDIO MUTE (H)
K602
9 LP (H)
R620
K601
7 BIAS CTL (H)
IC801 39PIN
BIAS CTL (H)
K601
4 PC 9V
PC 9V
K601
REC (H) 6
BIAS CTL
9V SW
Q8801
Q8809
AX
CC
15 BIAS CTL 9V 15

AUDIO BLOCK DIAGRAM
(FOR 2-HEAD MODELS) : VC-A30/A35/A40/A45 SERIES



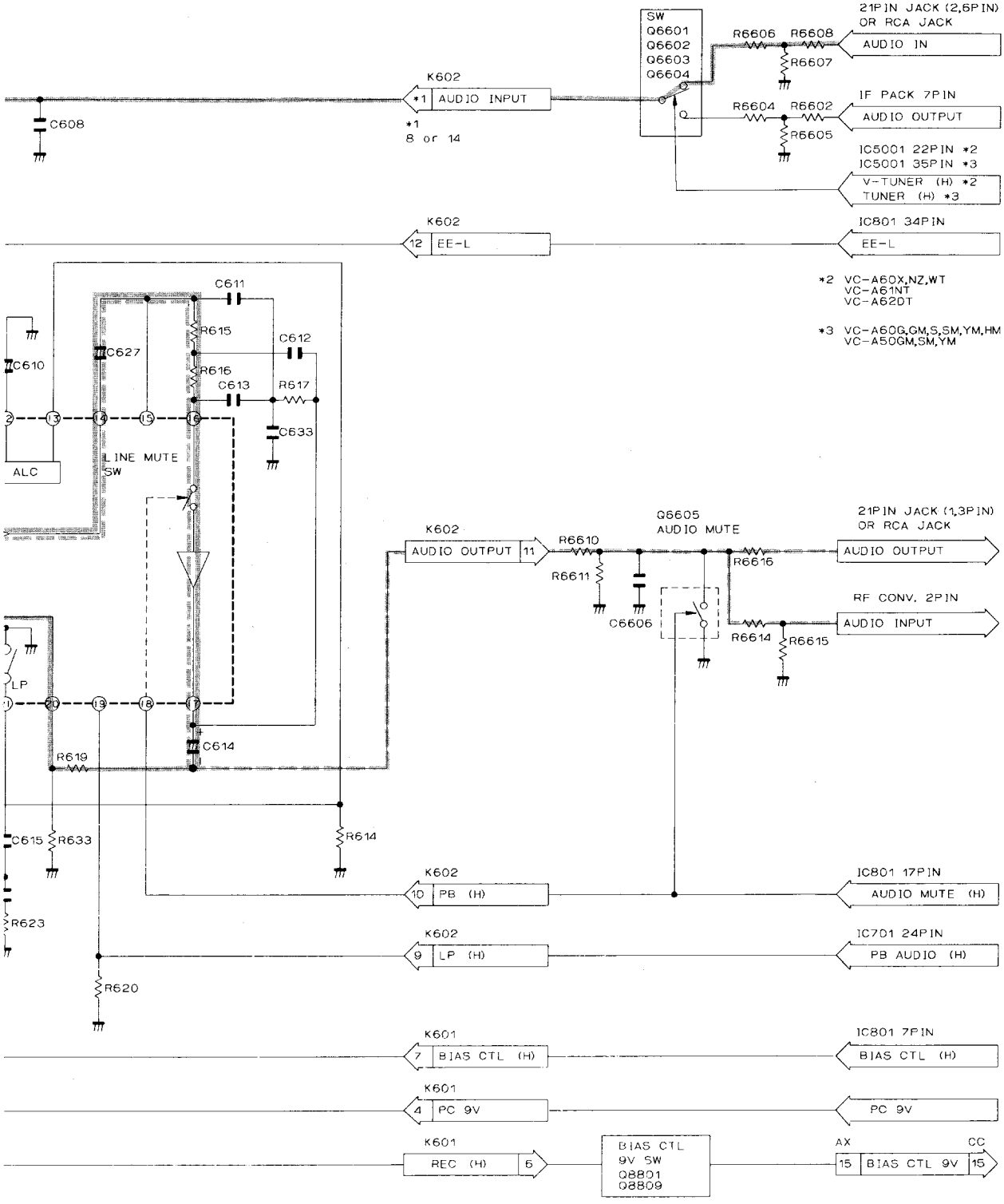

AUDIO PLAYBACK
AUDIO RECORDING
D.D. SYLINDER
FULL ERASE HEAD
AUDIO ERASE HEAD
AC HEAD
CONTROL SIGNAL
PINCHI ROLLER
REC
PB
TAPE
DRUM FG
FG
DRUM PG
PG
CAPSTAN SHAFT
CAPSTAN D.D. MOTOR
SERVO PROCESSOR
REF PERIOD GEN.
PHASE COMPARATOR
ADDER
AN
6 DRUM CTL
DRUM MOTOR DRIVE
3 AT12V
FREQUENCY DISCRIMINATOR
REC ON
PB
REC
HEAD(+)
AM
11 CAPSTAN CTL
CAPSTAN MOTOR DRIVE
13 AT12V
MECHANISM CONTROL SIGNAL
CIRCUIT CONTROL SIGNAL
SYSTEM CONTROL
CAPSTAN FG
PB
REC
CONTROL SIGNAL

AUDIO BLOCK DIAGRAM
(FOR 2-HEAD MODELS) : VC-A10 SERIES

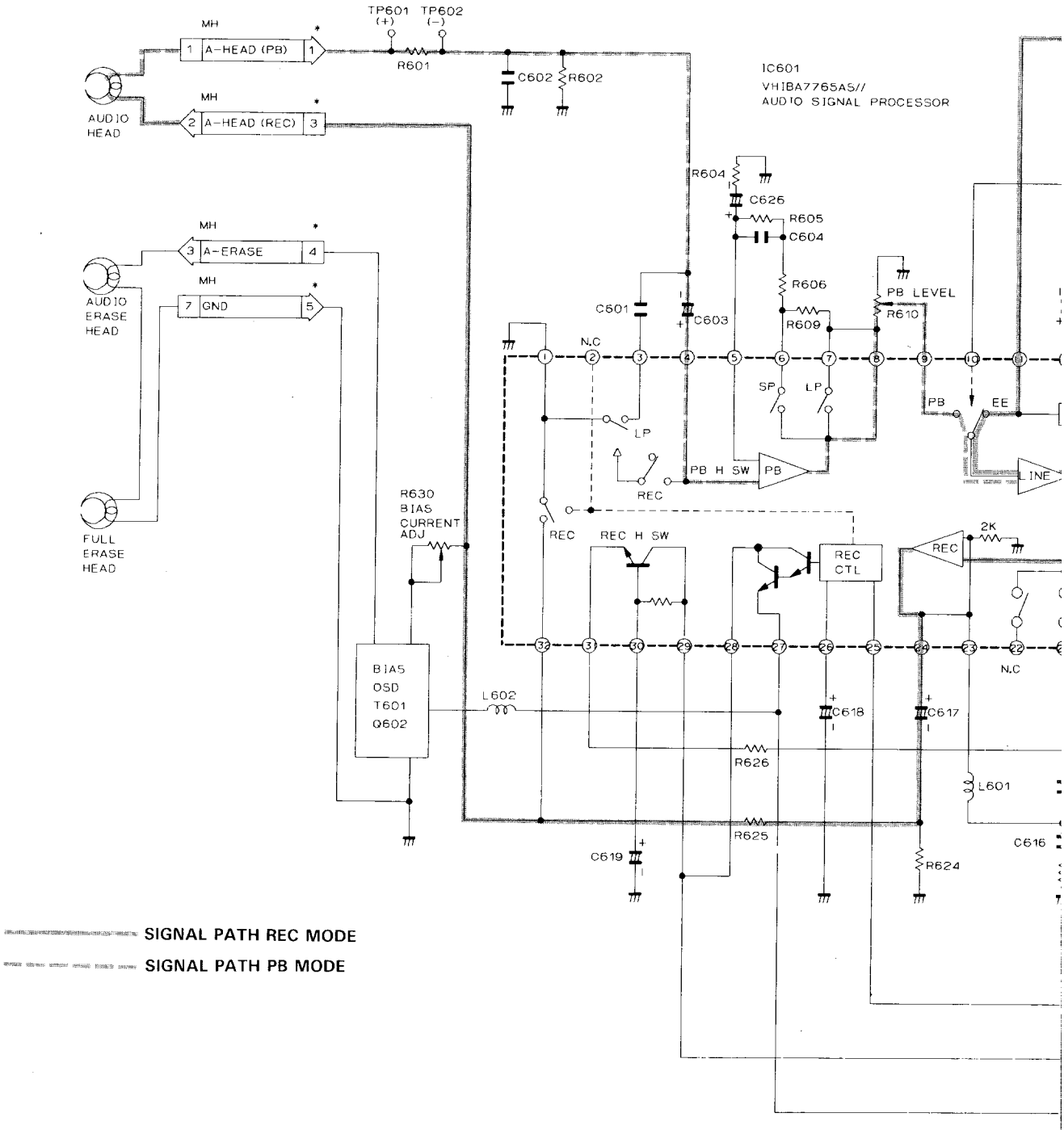


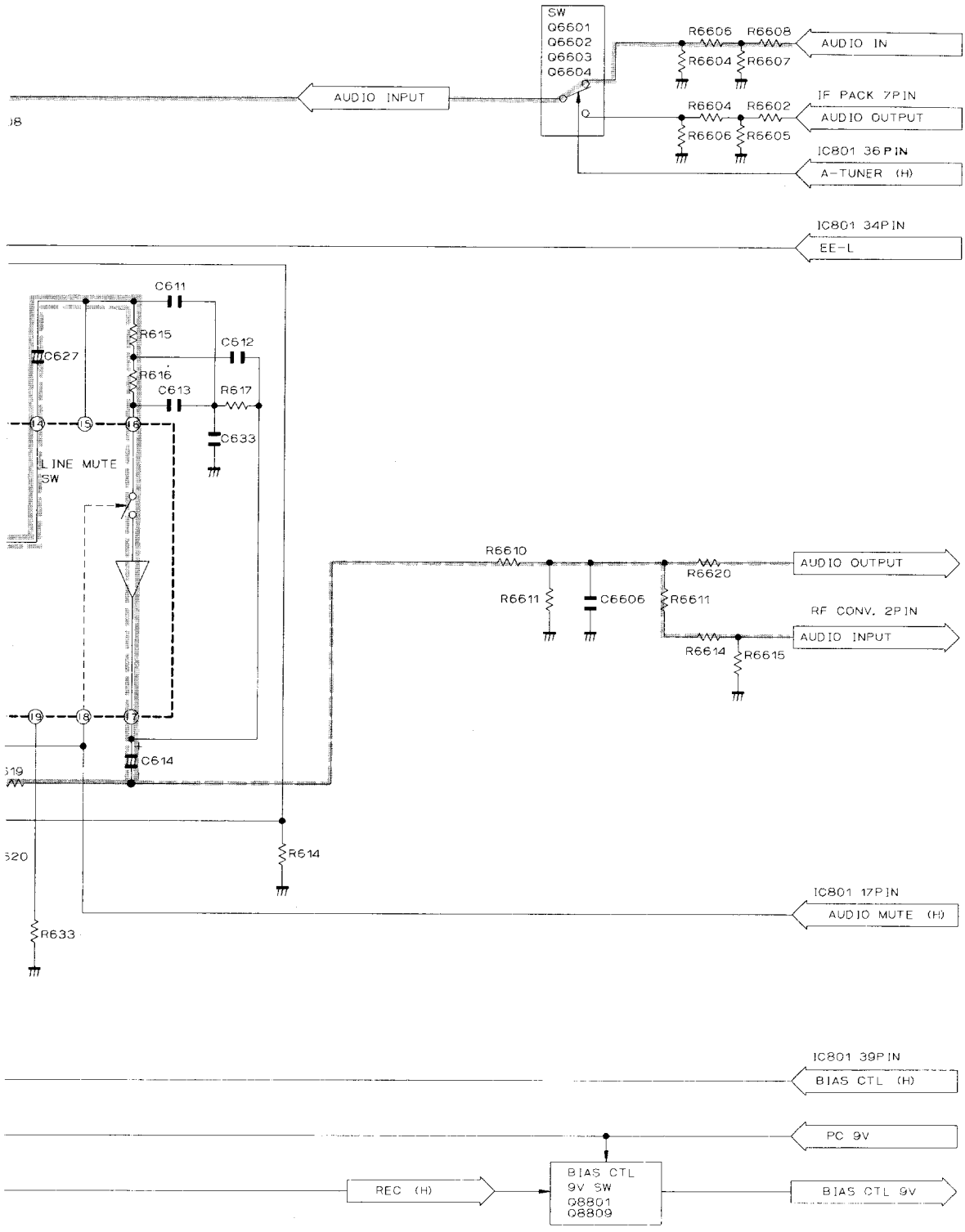
SIGNAL PATH REC MODE

SIGNAL PATH PB MODE

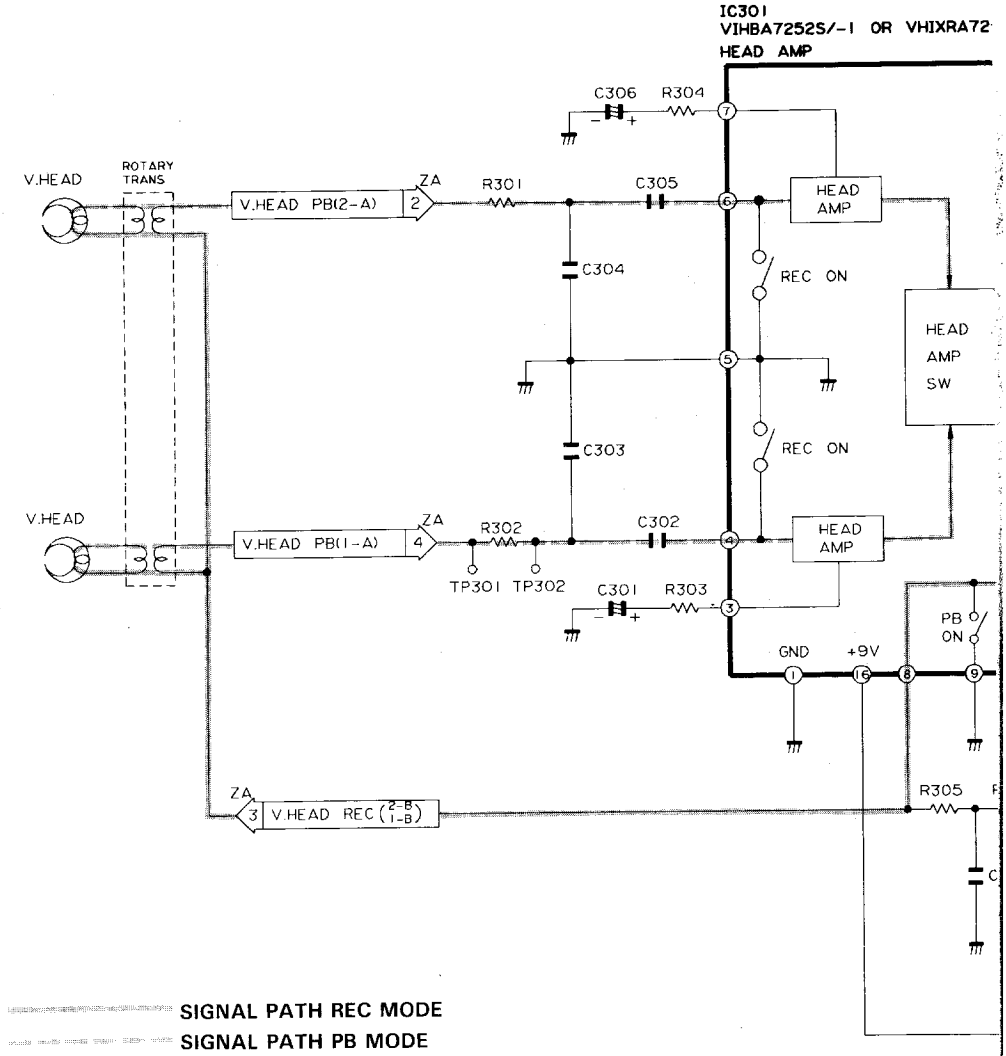

SW
Q6601
Q6602
Q6603
Q6604
21PIN JACK (2,6PIN)
OR RCA JACK
AUDIO IN
R6606
R6608
R6607
K602
*1
AUDIO INPUT
C608
*1
8 or 14
IF PACK 7PIN
AUDIO OUTPUT
R6604
R6602
R6605
IC5001 22PIN *2
IC5001 35PIN *3
V-TUNER (H) *2
TUNER (H) *3
K602
12
EE-L
IC801 34PIN
EE-L
*2 VC-A60X,NZ,WT
VC-A61NT
VC-A62DT
*3 VC-A60G,GM,S,SM,YM,HM
VC-A50GM,SM,YM
C611
R615
C612
C610
C627
R616
C613
R617
C633
ALC
LINE MUTE
SW
Q6605
AUDIO MUTE
21PIN JACK (1,3PIN)
OR RCA JACK
K602
AUDIO OUTPUT
11
R6610
R6611
C6606
R6616
AUDIO OUTPUT
RF CONV. 2PIN
AUDIO INPUT
R6614
R6615
LP
C614
R619
C615
R633
R614
R623
K602
10
PB (H)
IC801 17PIN
AUDIO MUTE (H)
K602
9
LP (H)
IC701 24PIN
PB AUDIO (H)
R620
K601
7
BIAS CTL (H)
IC801 7PIN
BIAS CTL (H)
K601
4
PC 9V
PC 9V
K601
REC (H)
6
BIAS CTL
9V SW
Q8801
Q8809
AX
CC
15
BIAS CTL 9V
15

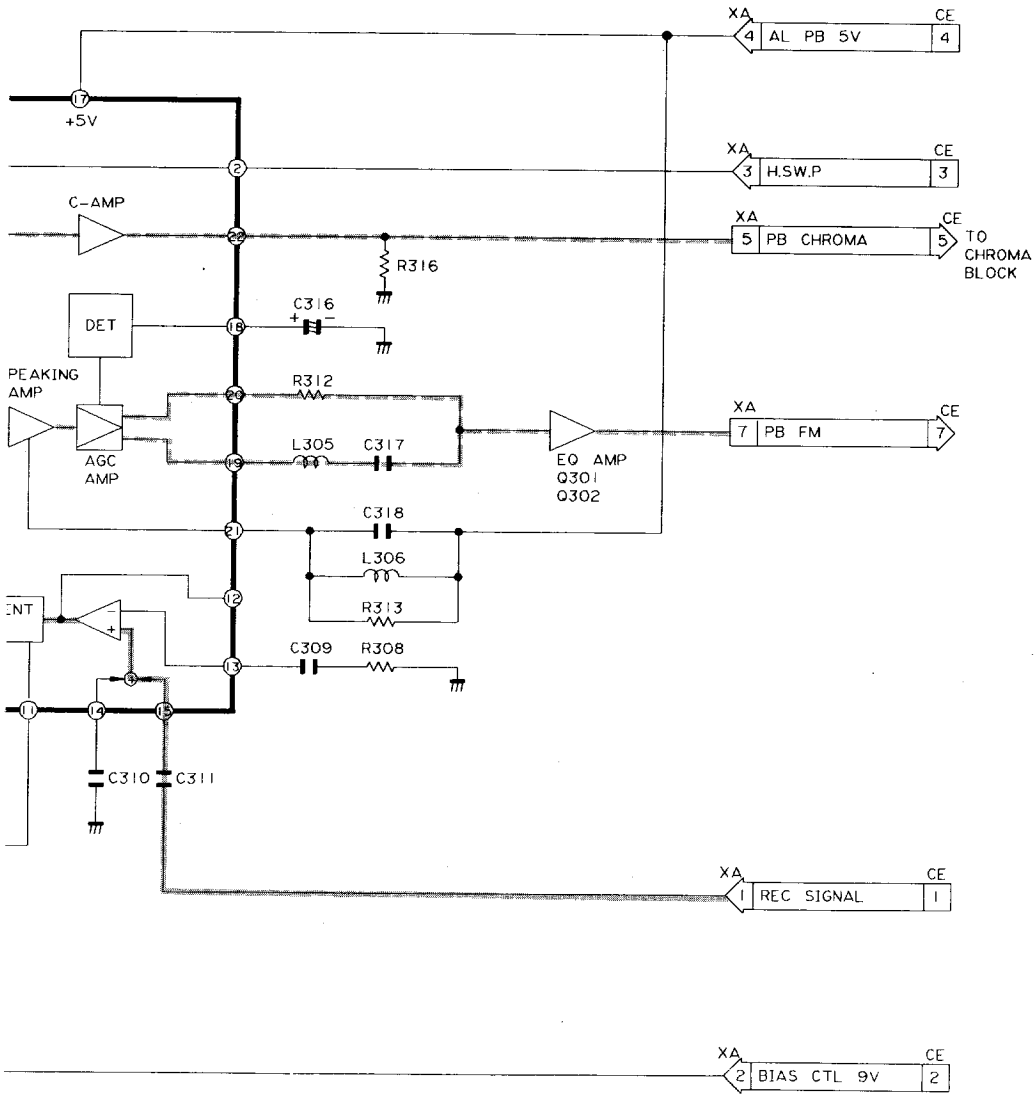
AUDIO BLOCK DIAGRAM
(FOR 4-HEAD MODELS) : VC-A50/A60/A61/A62 SERIES



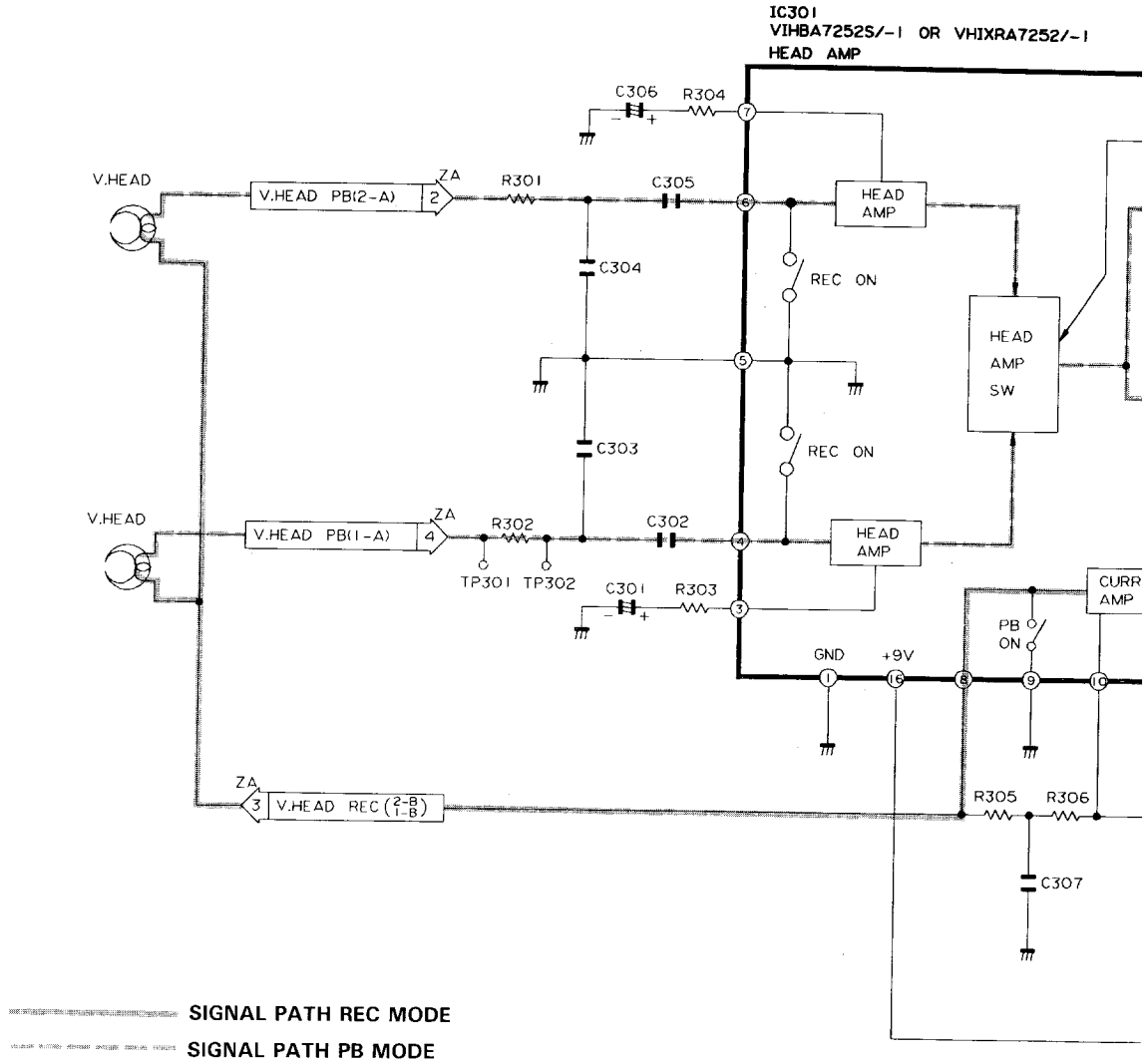

SW
Q6601
Q6602
Q6603
Q6604
R6606
R6608
AUDIO IN
R6604
R6607
AUDIO INPUT
IF PACK 7PIN
R6604
R6602
AUDIO OUTPUT
R6606
R6605
IC801 36PIN
A-TUNER (H)
IC801 34PIN
EE-L
C611
R615
C612
C627
R616
C613
R617
C633
LINE MUTE
SW
R6610
R6620
AUDIO OUTPUT
R6611
C6606
R6611
RF CONV. 2PIN
AUDIO INPUT
R6614
R6615
C614
R614
IC801 17PIN
AUDIO MUTE (H)
R633
IC801 39PIN
BIAS CTL (H)
PC 9V
REC (H)
BIAS CTL
9V SW
Q8801
Q8809
BIAS CTL 9V

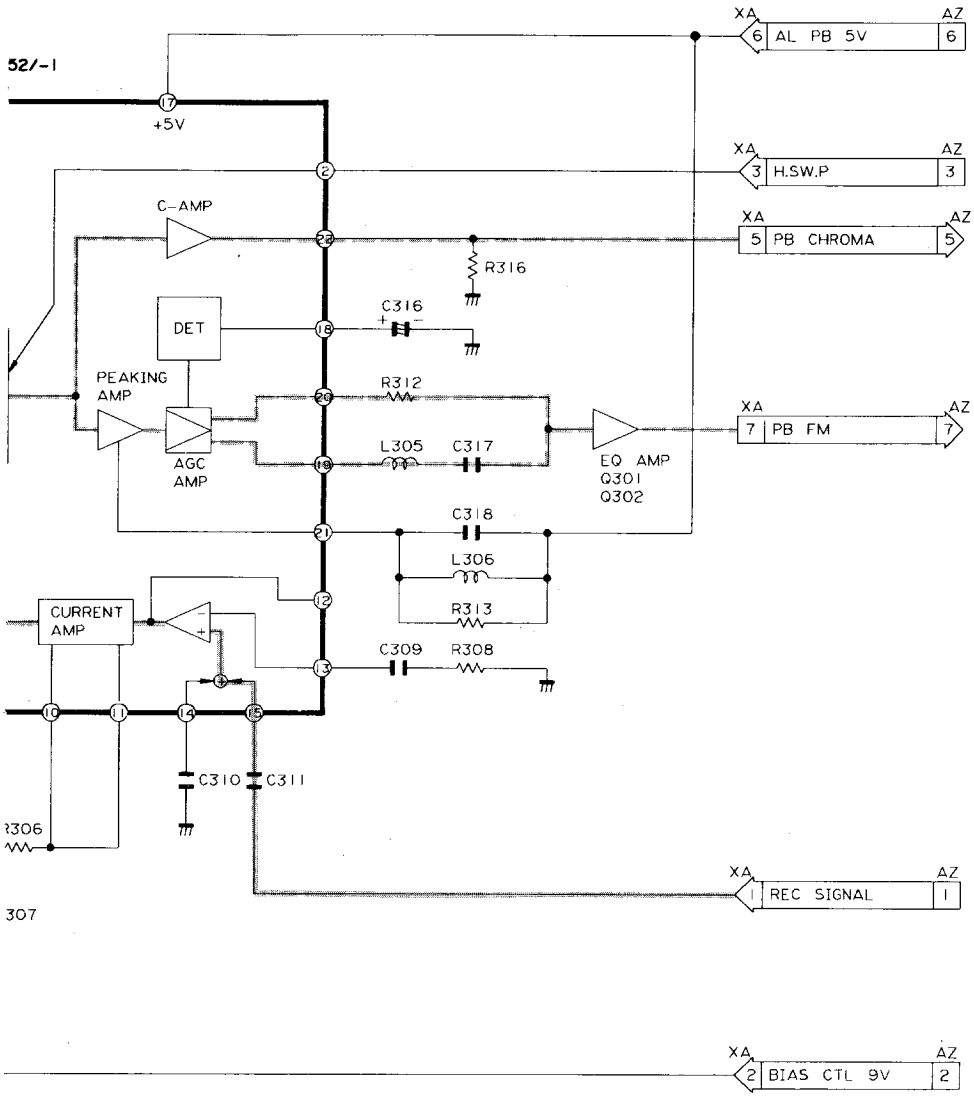
HEAD AMP BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES



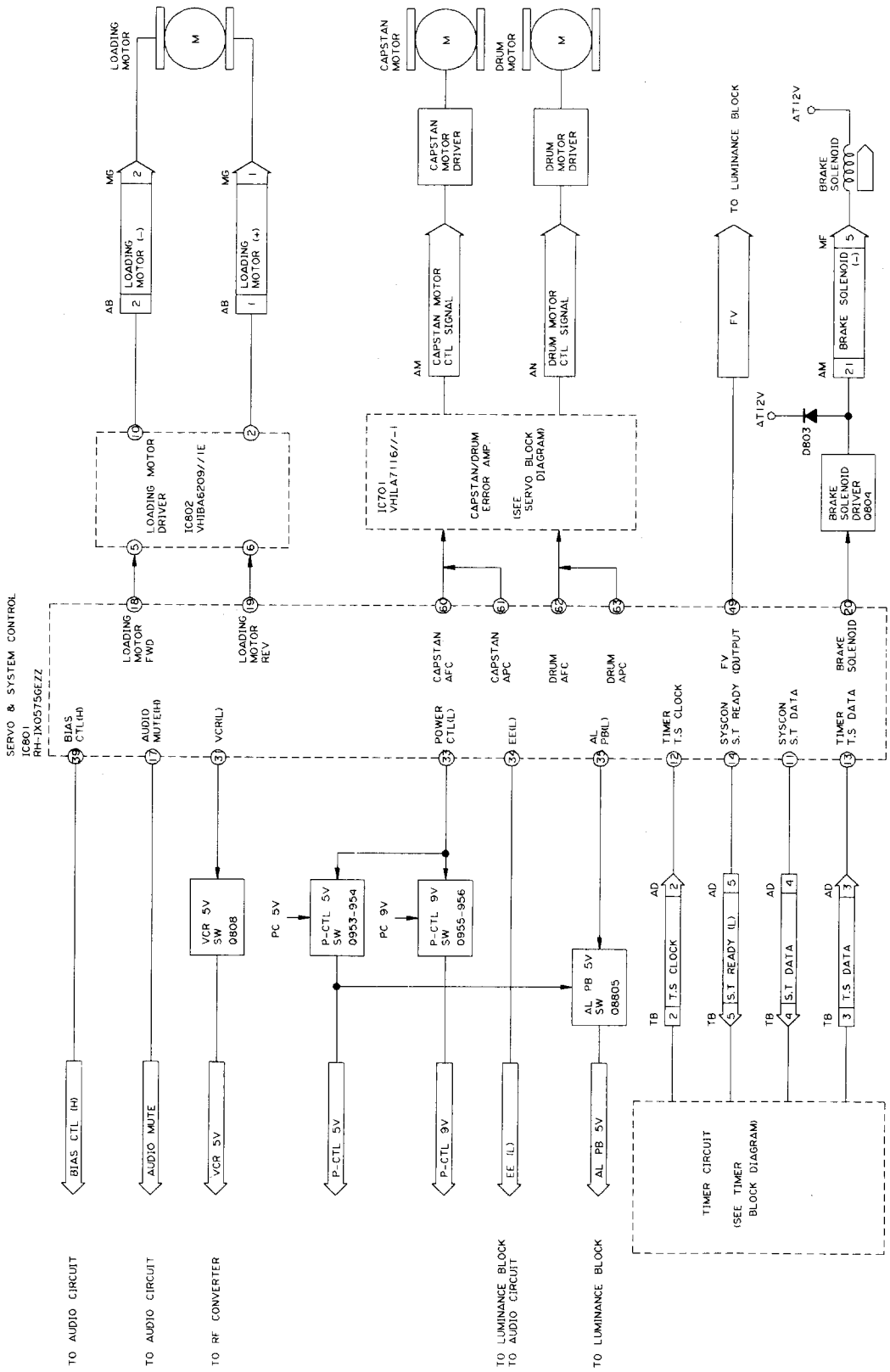

XA
CE
4 AL PB 5V 4
17
+5V
2
XA
3 H.SW.P 3
C-AMP
20
XA
5 PB CHROMA 5
TO CHROMA BLOCK
R316
C316
DET
18
PEAKING AMP
R312
XA
7 PB FM 7
L305
C317
AGC AMP
19
EQ AMP Q301 Q302
C318
21
L306
12
R313
C309
R308
13
11
14
15
C310
C311
XA
1 REC SIGNAL 1
XA
2 BIAS CTL 9V 2

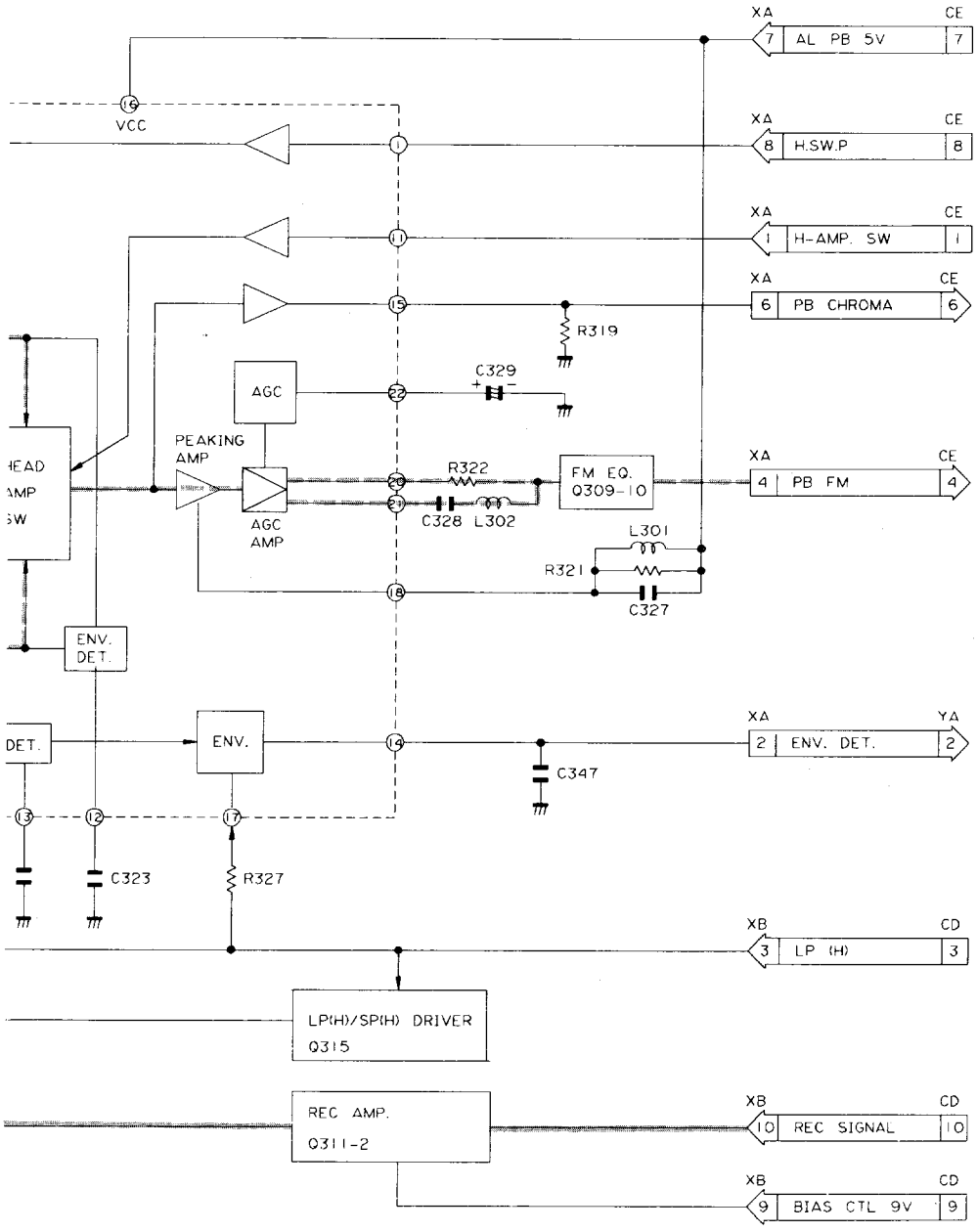
HEAD AMP BLOCK DIAGRAM
(FOR 2-HEAD MODELS) : VC-A30/A35/A40/A45 SERIES



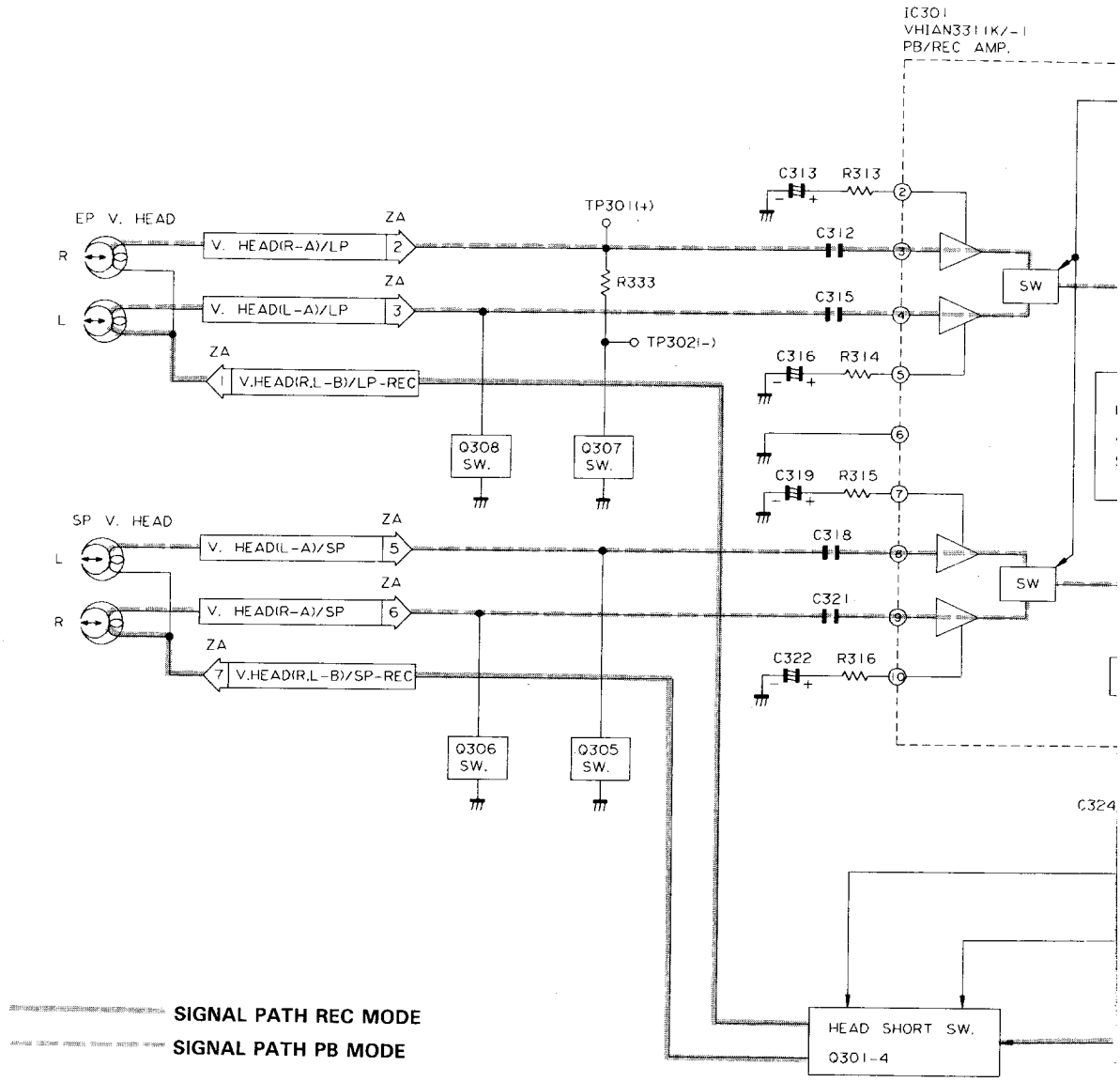

52/-1
+5V
C-AMP
DET
PEAKING AMP
AGC AMP
R316
C316
R312
L305
C317
EQ AMP
Q301
Q302
C318
L306
R313
CURRENT AMP
C309
R308
C310
C311
3306
307
XA
AZ
6 AL PB 5V 6
3 H.SW.P 3
5 PB CHROMA 5
7 PB FM 7
1 REC SIGNAL 1
2 BIAS CTL 9V 2

SYSTEM CONTROL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A30/A35/A40/A45 SERIES

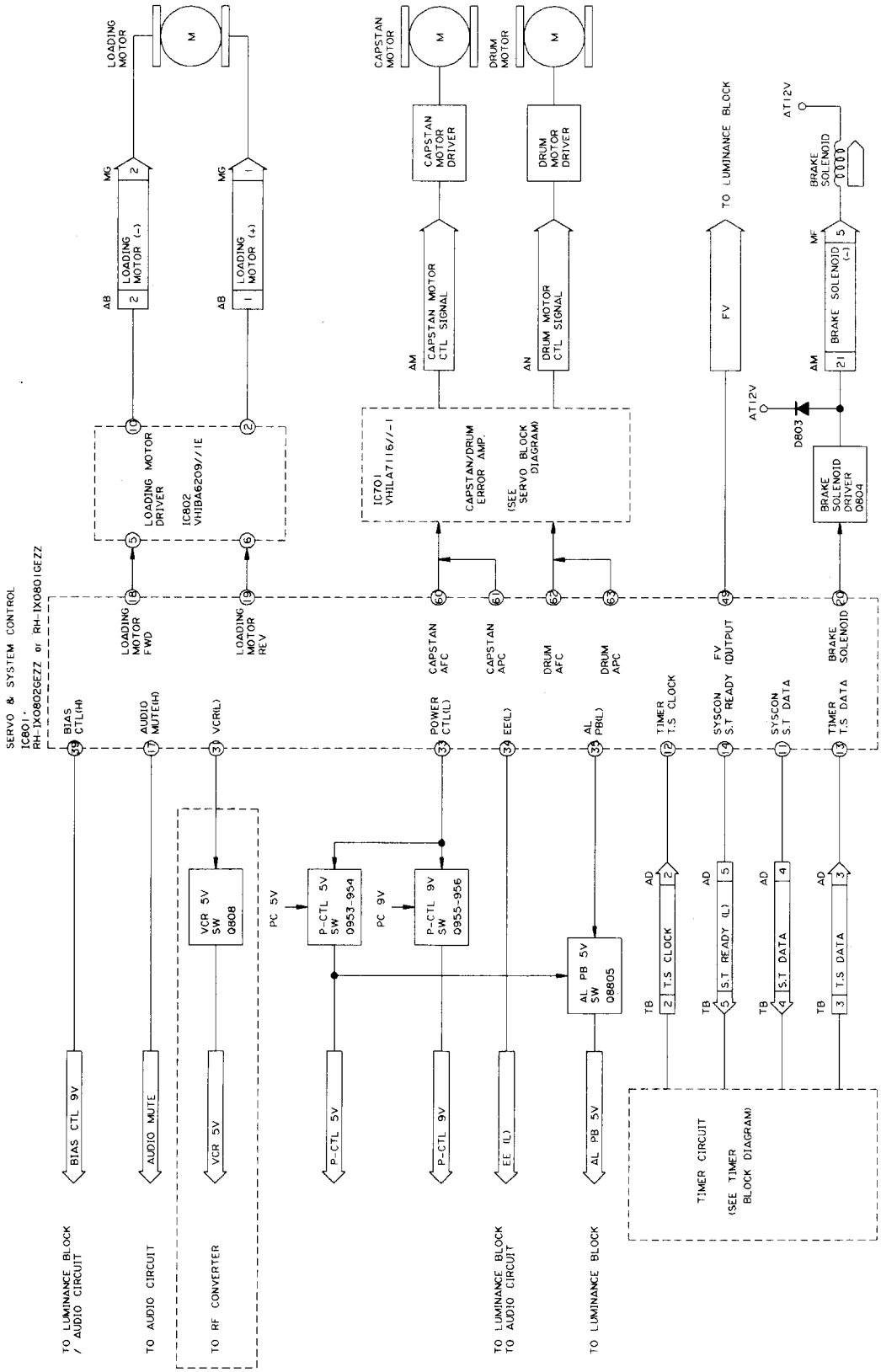



XA
CE
7
AL PB 5V
7
VCC
16
XA
CE
8
H.SW.P
8
1
XA
CE
1
H-AMP. SW
1
11
XA
CE
6
PB CHROMA
6
15
R319
C329
AGC
22
PEAKING
AMP
R322
FM EQ.
Q309-10
XA
CE
4
PB FM
4
20
21
C328
L302
AGC
AMP
L301
R321
C327
18
ENV.
DET.
XA
YA
2
ENV. DET.
2
ENV.
14
C347
13
12
17
C323
R327
XB
CD
3
LP (H)
3
LP(H)/SP(H) DRIVER
Q315
REC AMP.
Q311-2
XB
CD
10
REC SIGNAL
10
XB
CD
9
BIAS CTL 9V
9

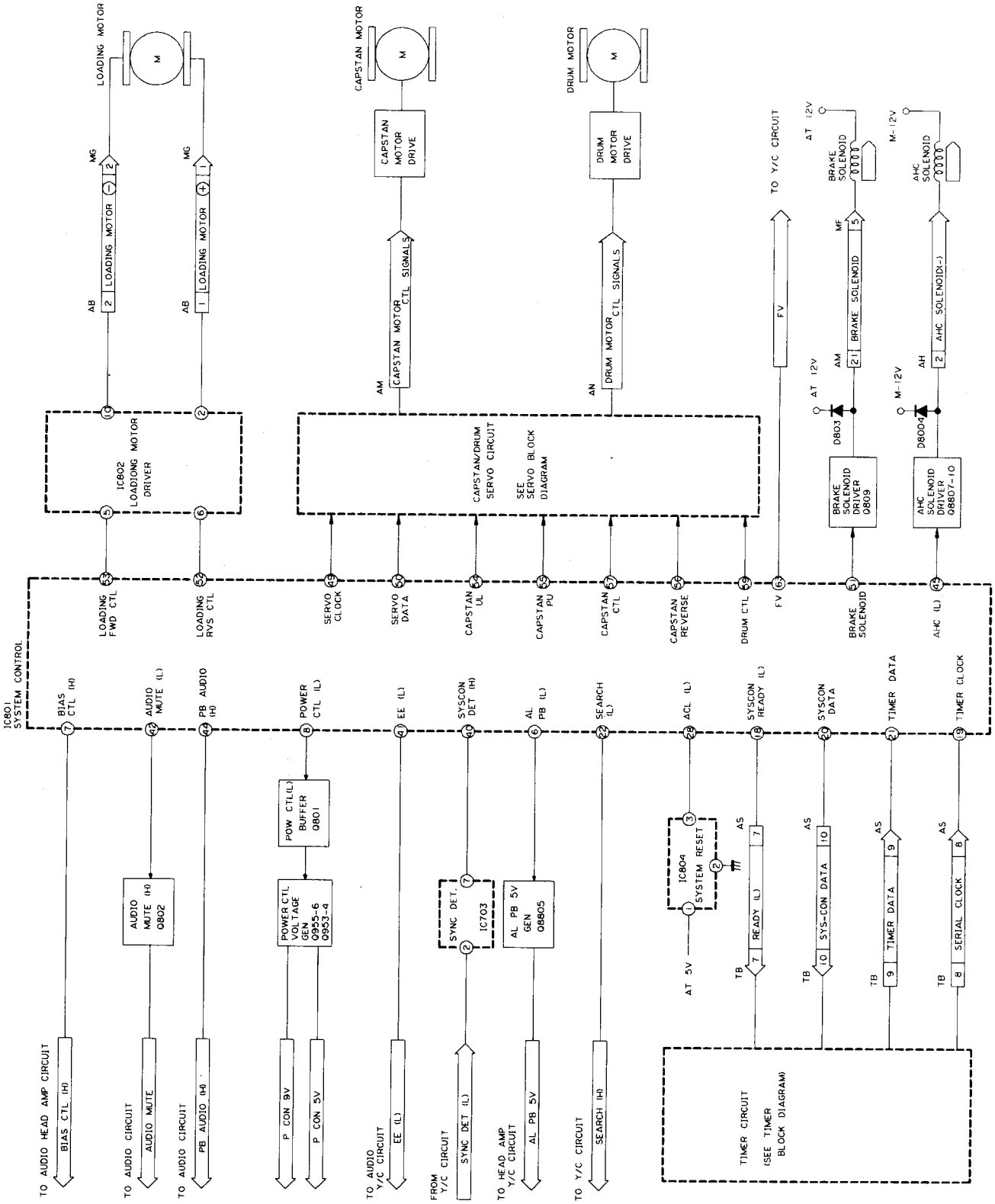
HEAD AMP BLOCK DIAGRAM
(FOR 4-HEAD MODELS) : VC-A50/A60/A61/A62 SERIES



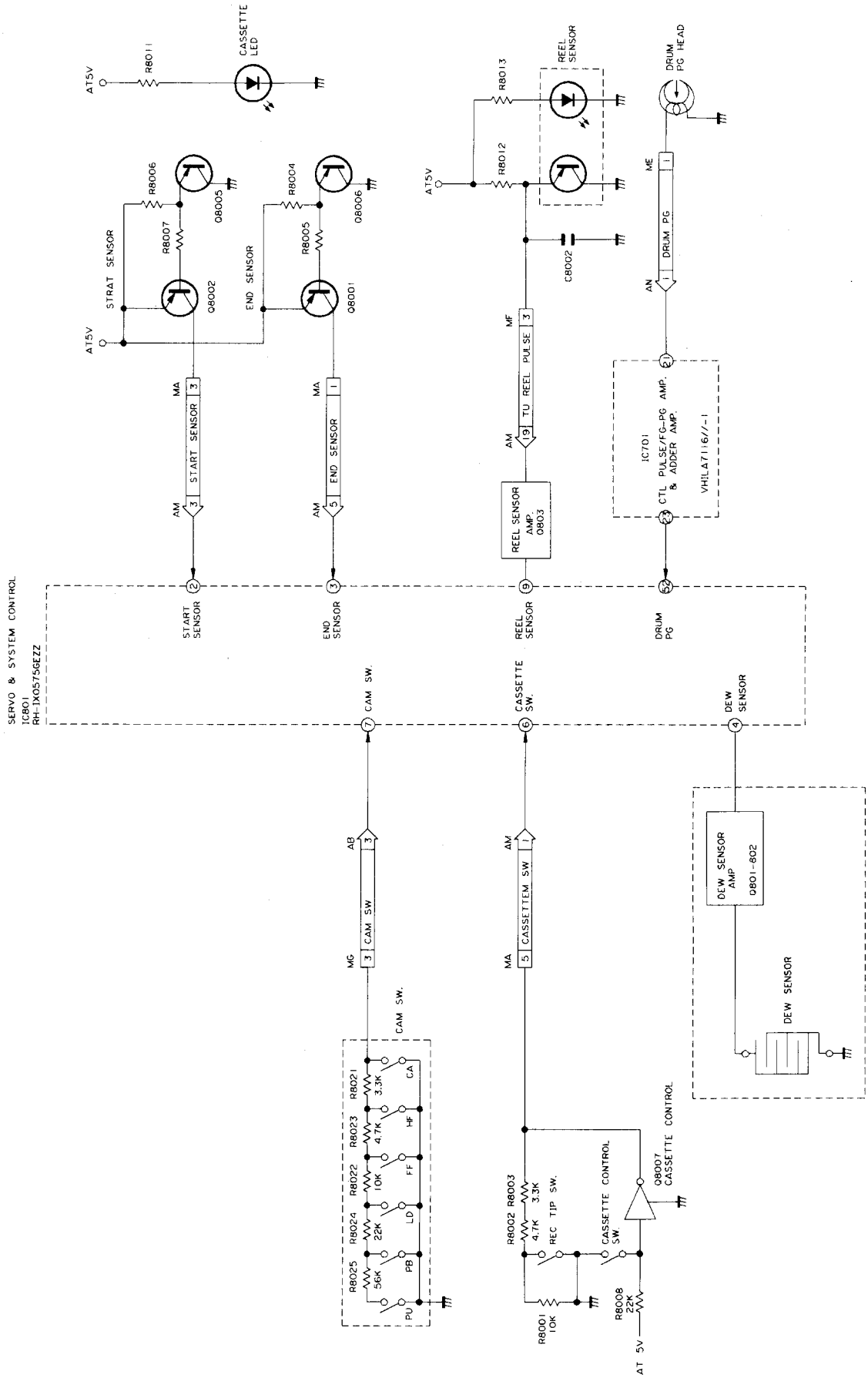
SYSTEM CONTROL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES



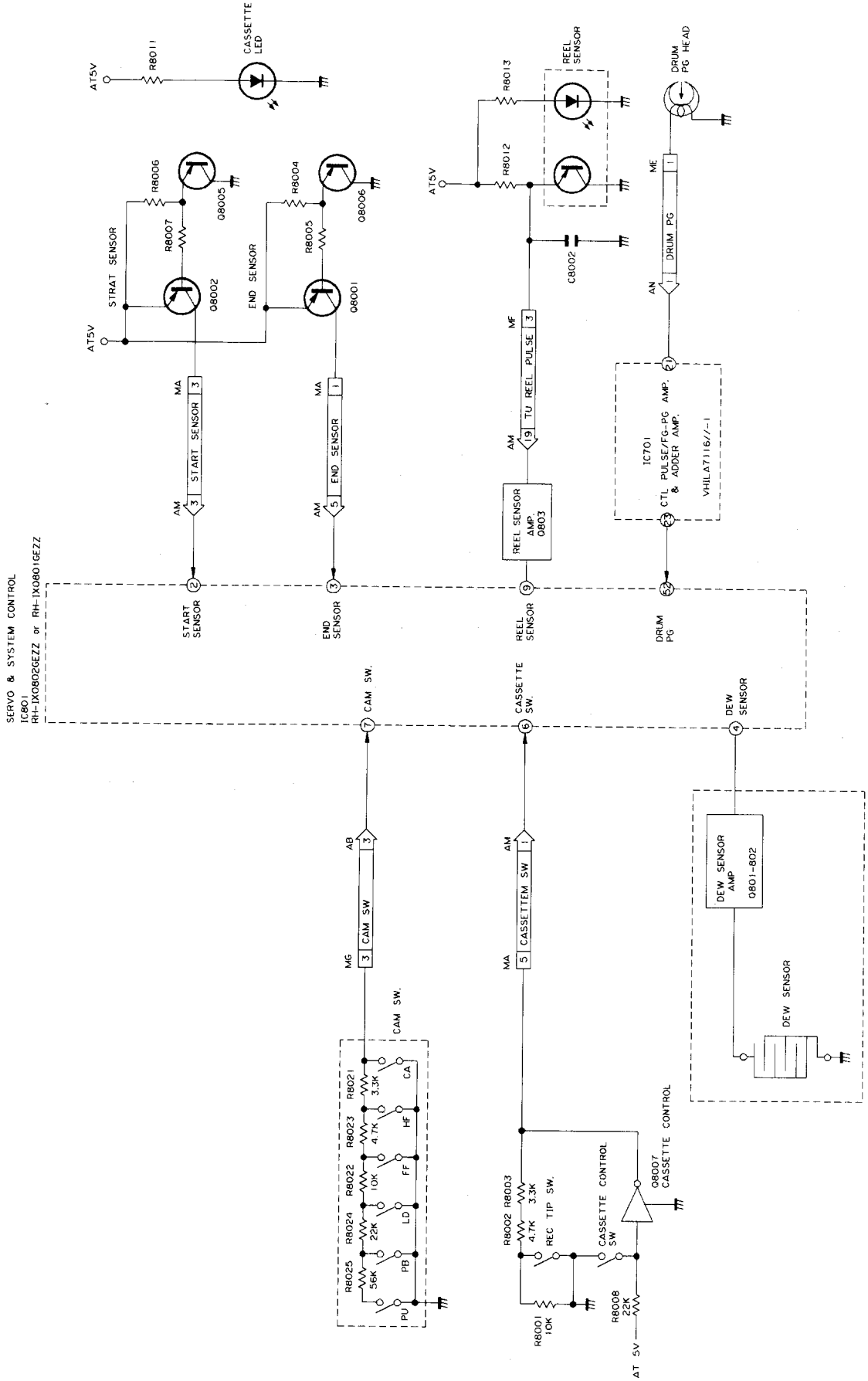
SYSTEM CONTROL BLOCK DIAGRAM (FOR 4-HEAD MODELS) : VC-A50/A60/A61/A62 SERIES



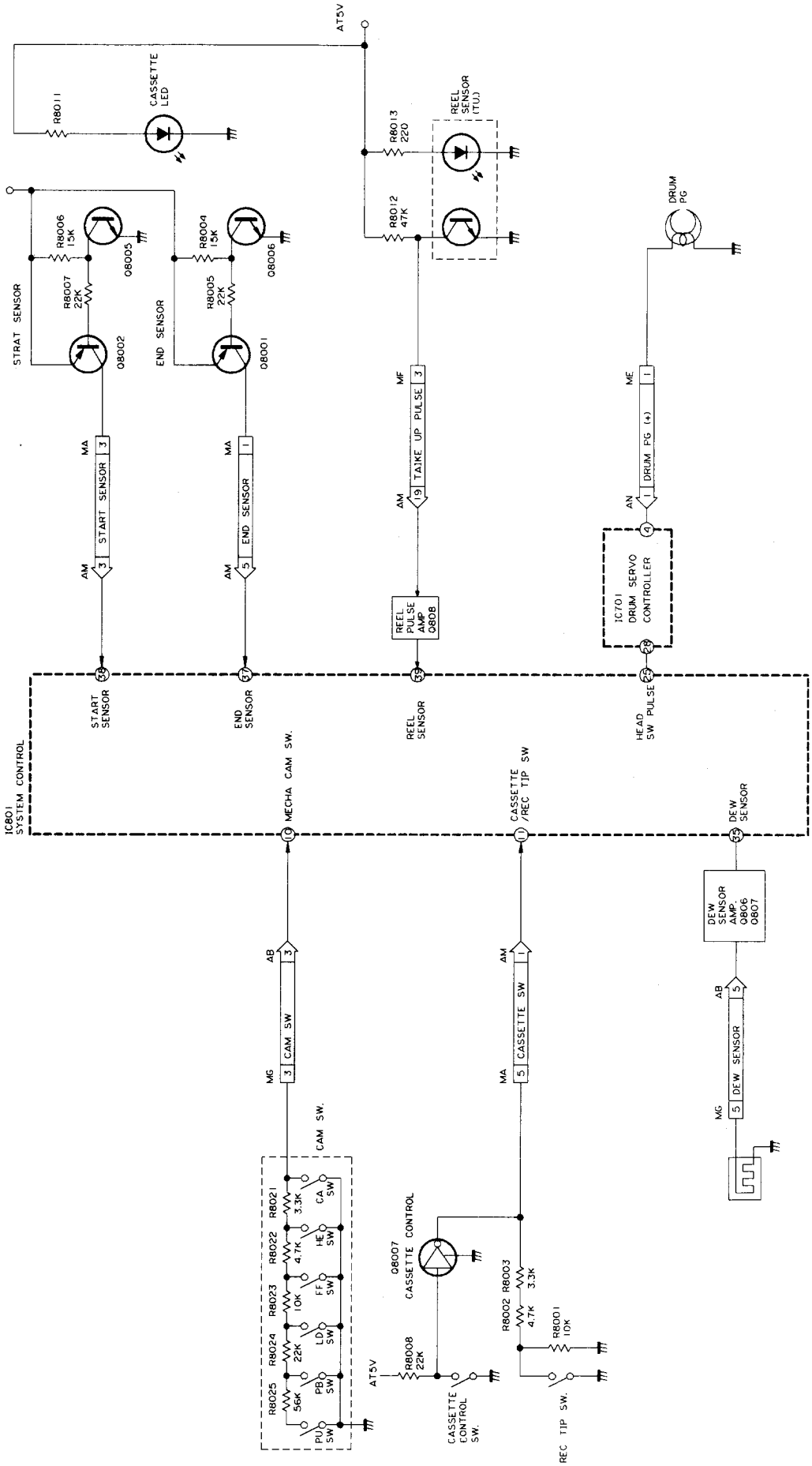
SAFETY DEVICE BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A30/A35/A40/A45 SERIES



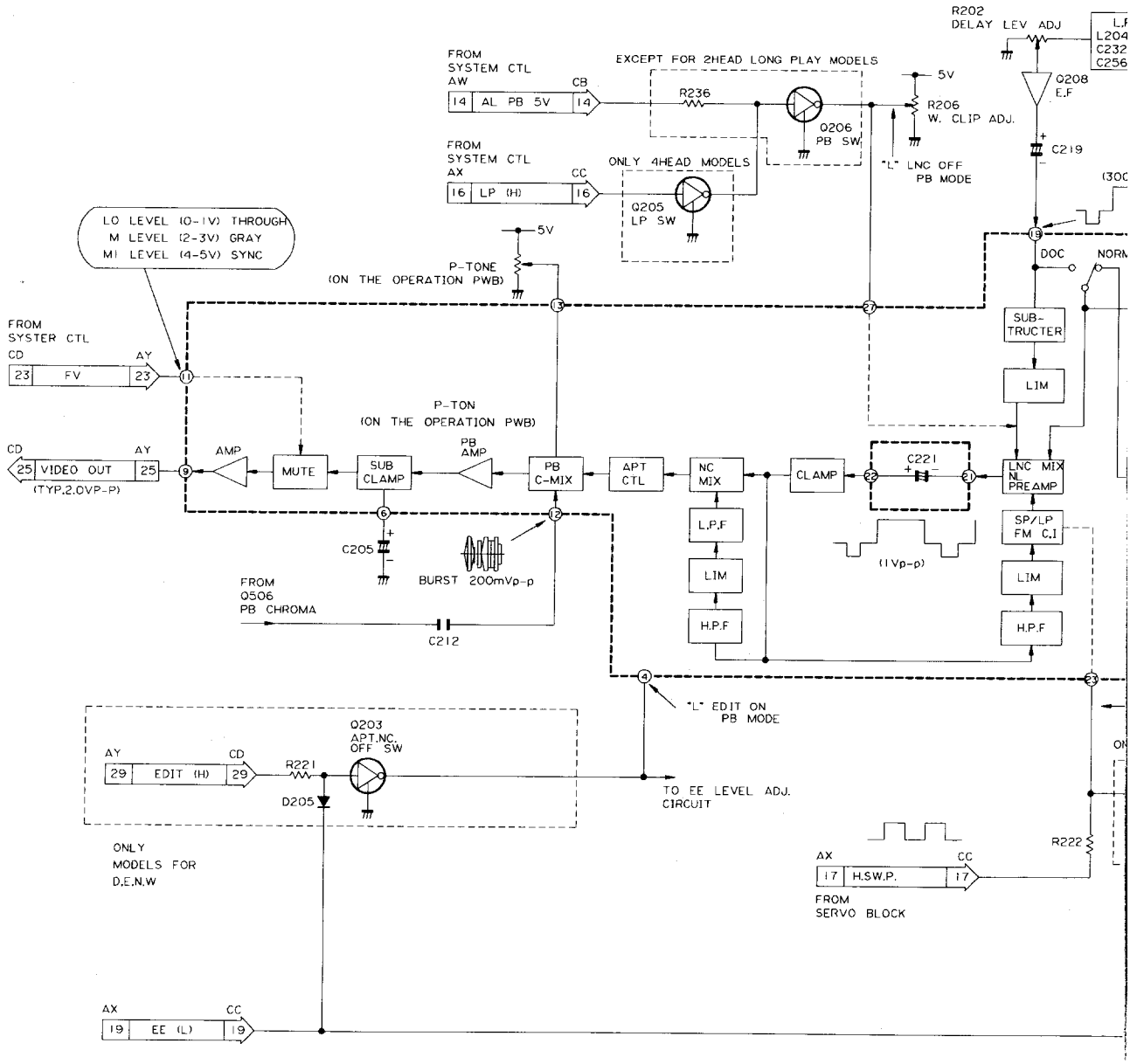
SAFETY DEVICE BLOCK DIAGRAM
(FOR 2-HEAD MODELS) : VC-A30G/GM/S/SM/SV, VC-A40G/GM/S/SM

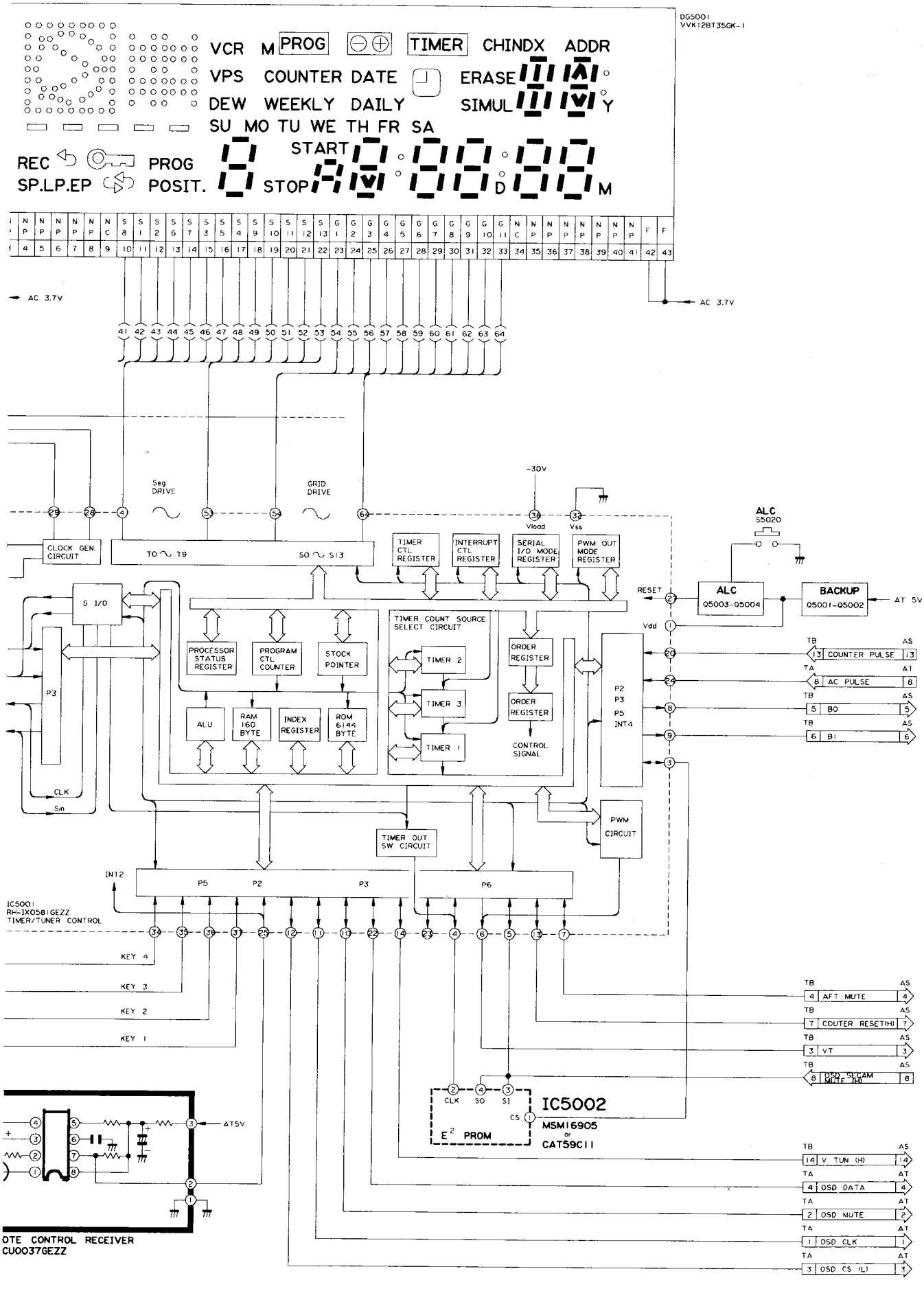


SAFETY DEVICE BLOCK DIAGRAM (FOR 4-HEAD MODELS) : VC-A50/A60/A61/A62 SERIES

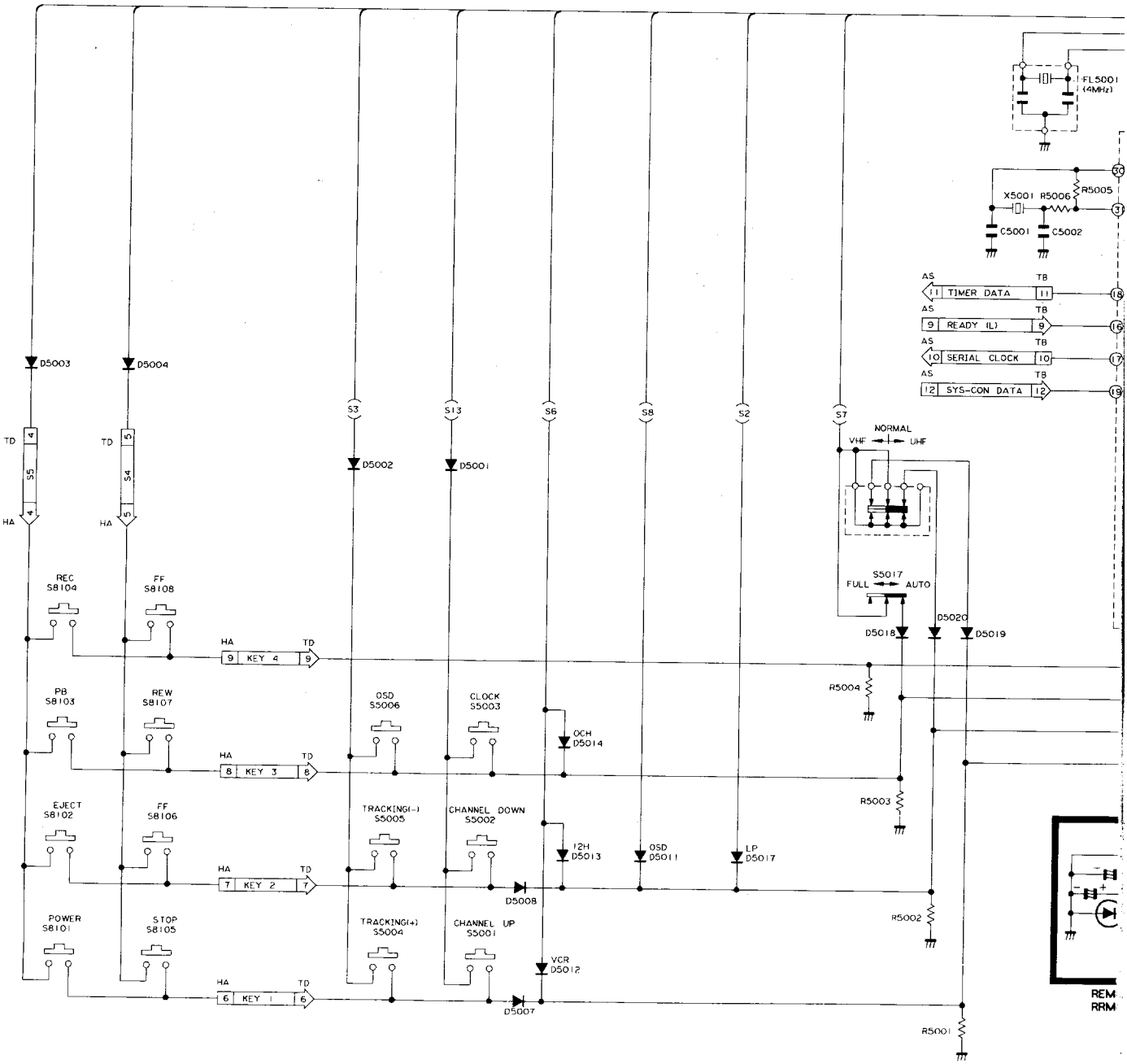


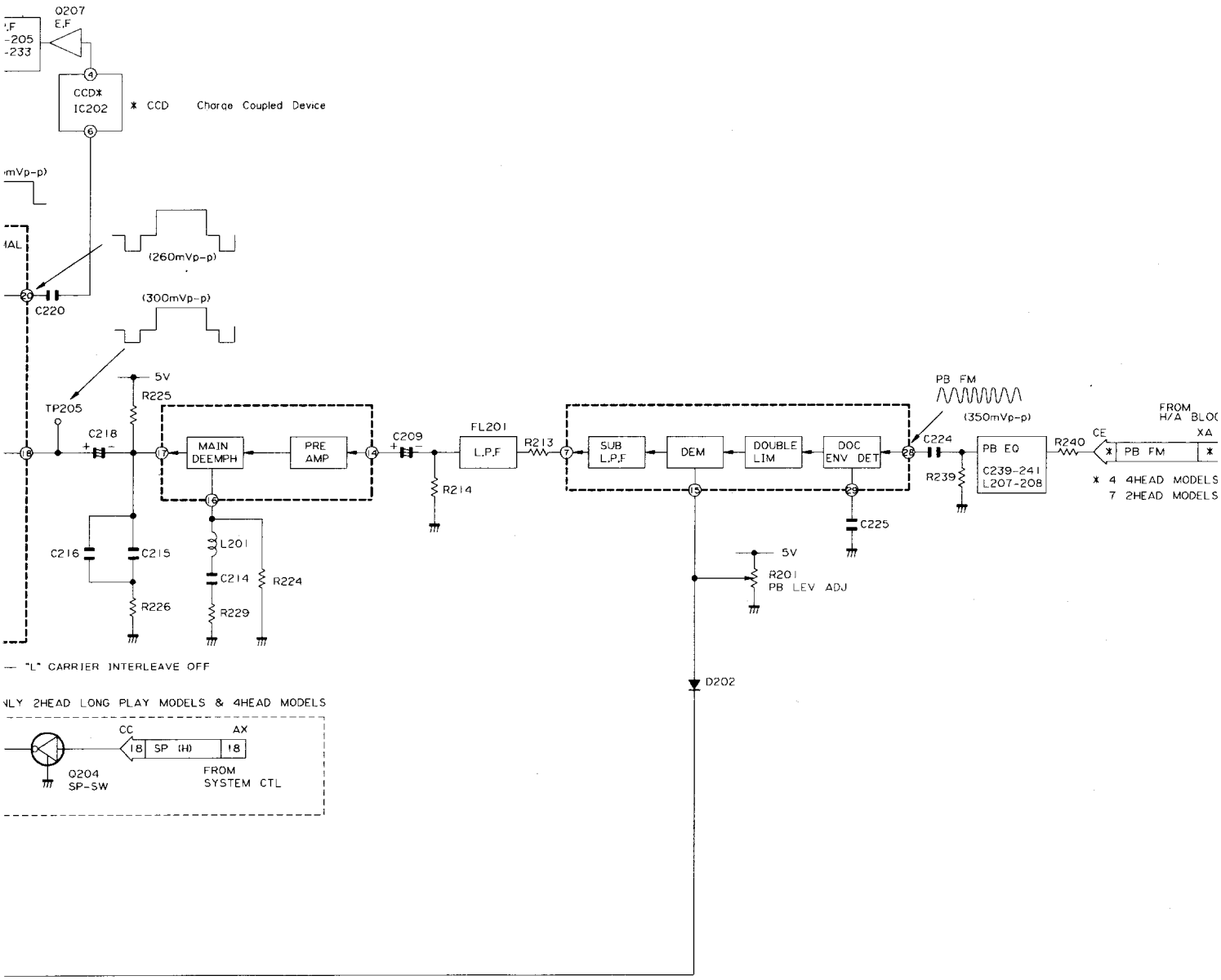
PB LUMINANCE SIGNAL BLOCK DIAGRAM
VC-A30/A35/A40/A45 SERIES
VC-A50/A60/A61/A62 SERIES



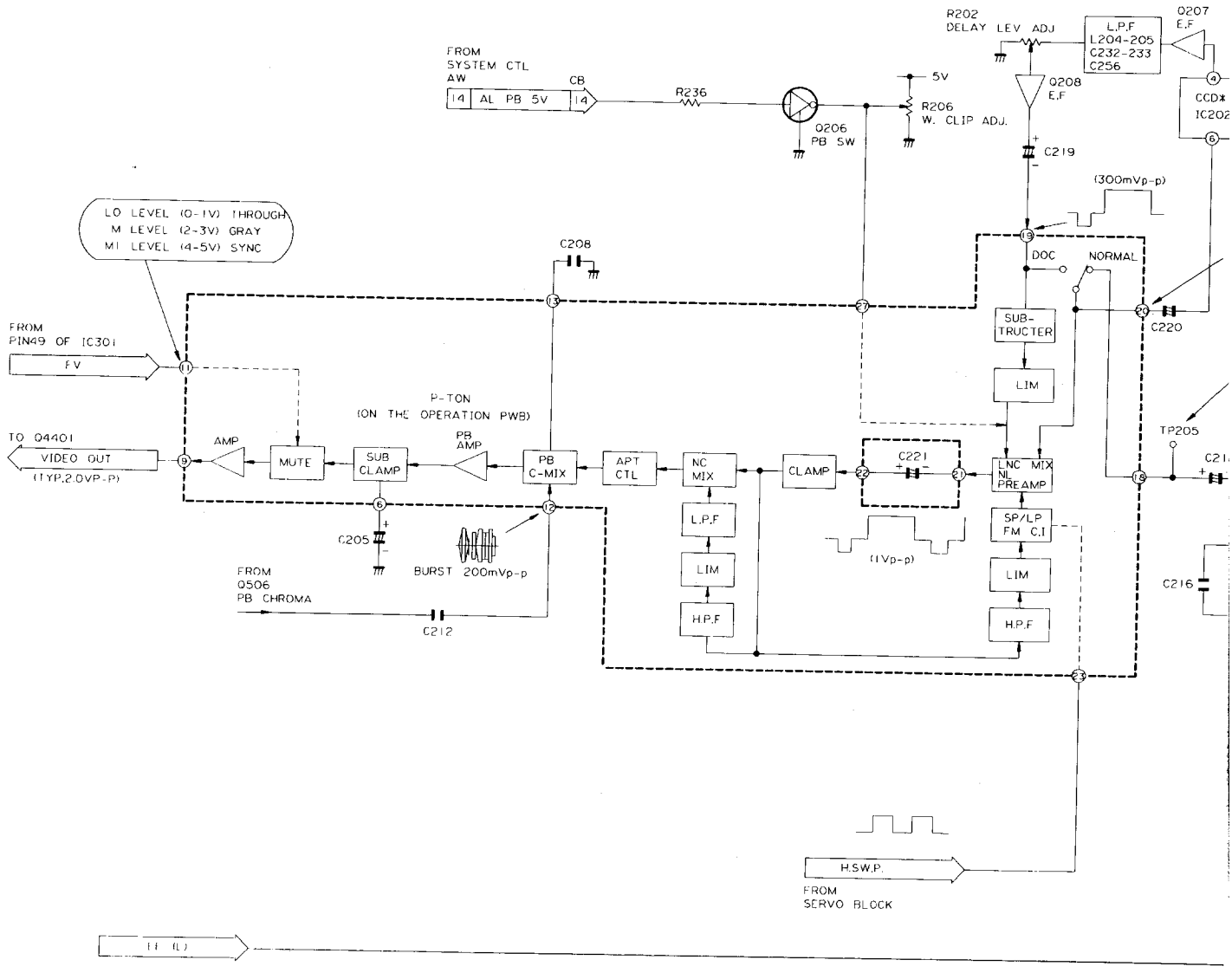

DG5001
VVK12BT35GK-1
VCR M PROG TIMER CHINDX ADDR
VPS COUNTER DATE ERASE
DEW WEEKLY DAILY SIMUL
SU MO TU WE TH FR SA
REC PROG
SP.LP.EP POSIT.
START
STOP
AM PM D M
AC 3.7V
Seg DRIVE
GRID DRIVE
-30V
Vload
Vss
CLOCK GEN. CIRCUIT
TO ~ T9
SO ~ S13
TIMER CTL REGISTER
INTERRUPT CTL REGISTER
SERIAL I/O MODE REGISTER
PWM OUT MODE REGISTER
ALC S5020
ALC Q5003-05004
BACKUP Q5001-05002
AT 5V
RESET
Vdd
S I/O
P3
CLK
Sin
PROCESSOR STATUS REGISTER
PROGRAM CTL COUNTER
STOCK POINTER
ALU
RAM 160 BYTE
INDEX REGISTER
ROM 6144 BYTE
TIMER COUNT SOURCE SELECT CIRCUIT
TIMER 2
TIMER 3
TIMER 1
ORDER REGISTER
ORDER REGISTER
CONTROL SIGNAL
P2
P3
P5
INT4
PWM CIRCUIT
TIMER OUT SW CIRCUIT
INT2
P5 P2 P3 P6
IC5001
RH-IX0581GEZZ
TIMER/TUNER CONTROL
KEY 4
KEY 3
KEY 2
KEY 1
TB AS
13 COUNTER PULSE 13
TA AT
8 AC PULSE 8
TB AS
5 BO 5
TB AS
6 BI 6
TB AS
4 AFT MUTE 4
TB AS
7 COUTER RESET(H) 7
TB AS
3 VT 3
TB AS
8 OSD SECAM MUTE (H) 8
CLK SO SI
CS
E2 PROM
IC5002
MSM16905
or
CAT59C11
TB AS
14 V TUN (H) 14
TA AT
4 OSD DATA 4
TA AT
2 OSD MUTE 2
TA AT
1 OSD CLK 1
TA AT
3 OSD CS (L) 3
AT5V
OTE CONTROL RECEIVER
CU0037GEZZ

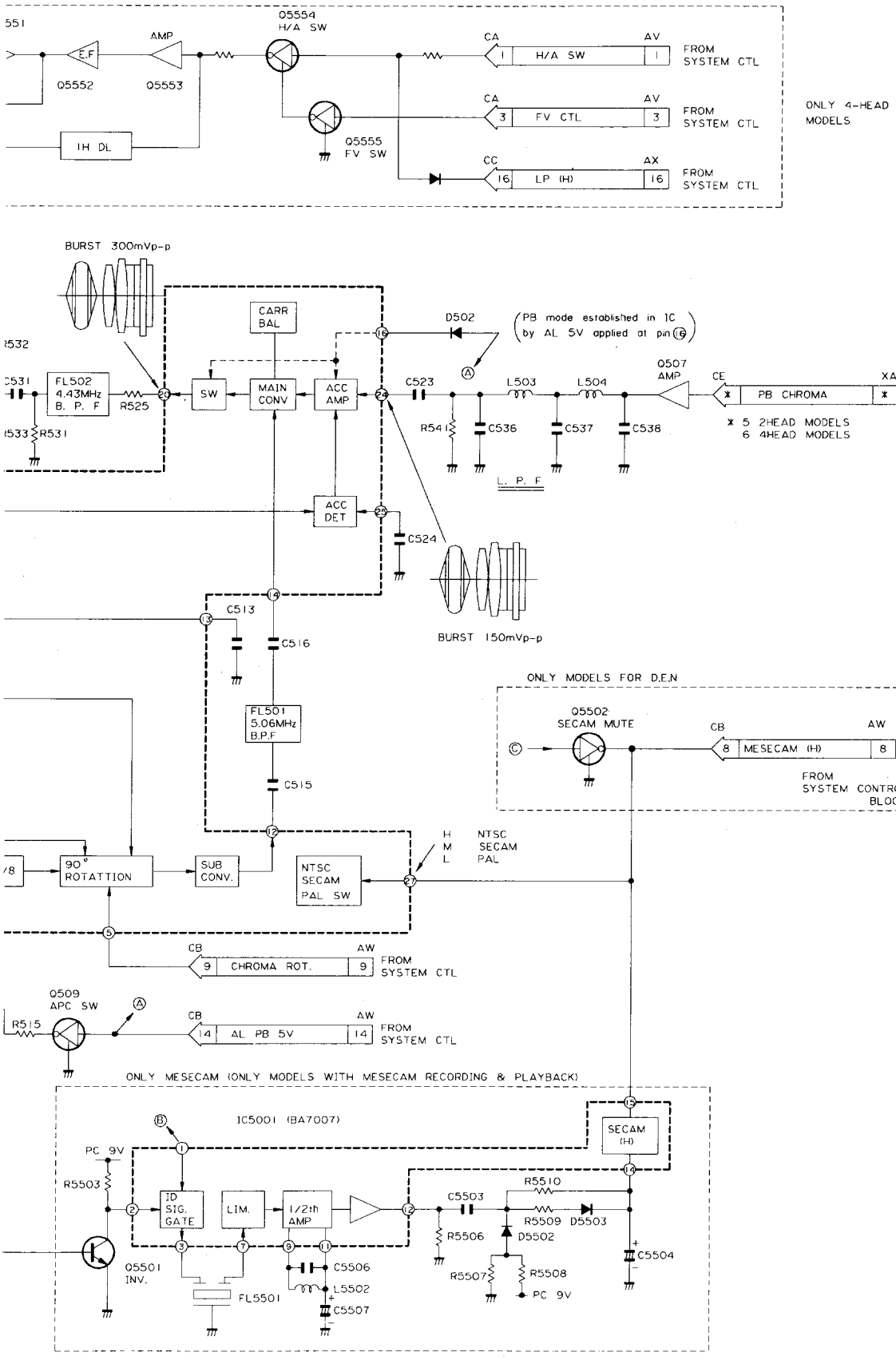
TIMER BLOCK DIAGRAM
(FOR 4-HEAD MODELS) : VC-A60/A61/A62 SERIES



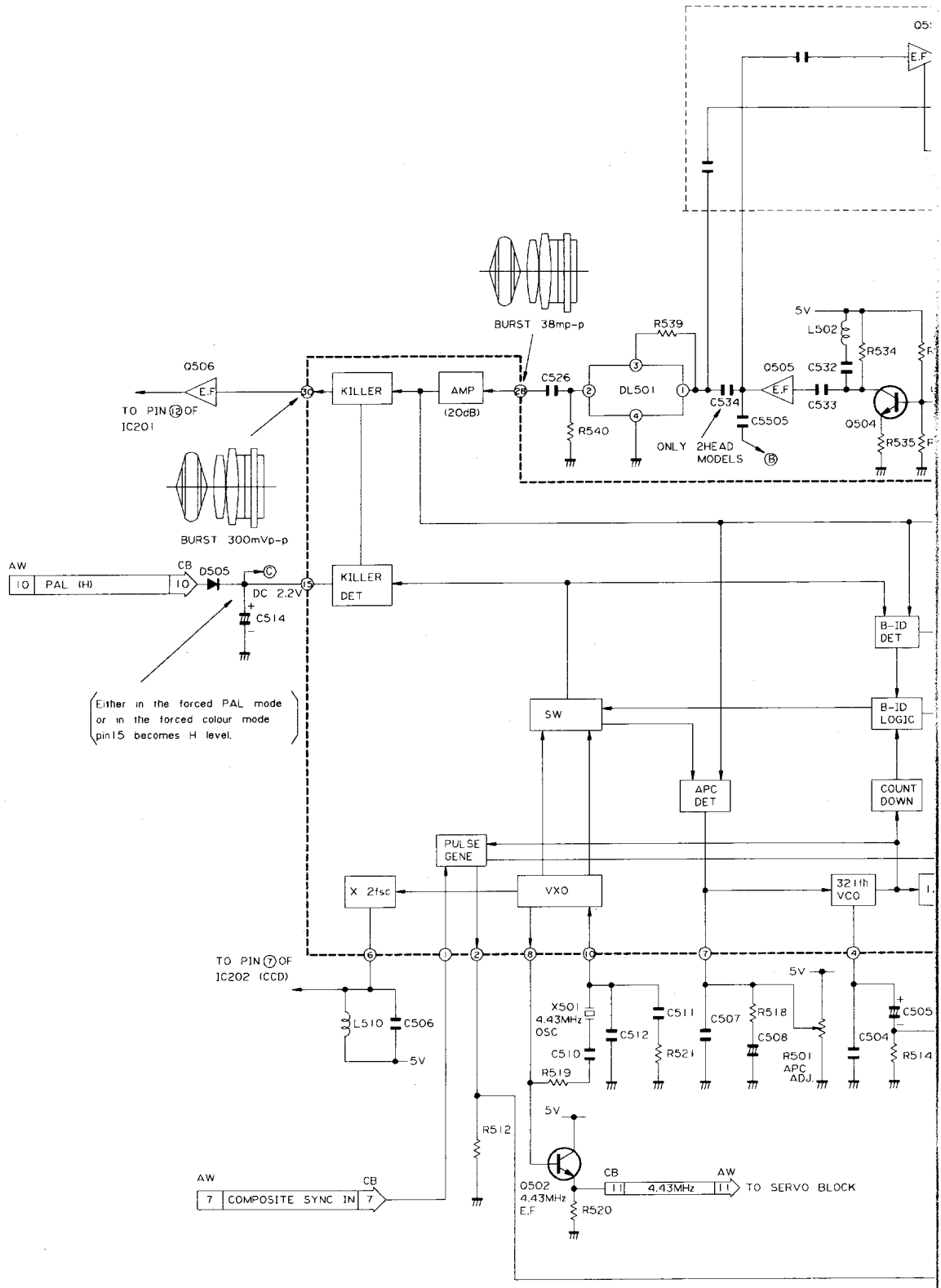

Q207
E.F
CCD*
IC202
* CCD Charge Coupled Device
(260mVp-p)
C220
(300mVp-p)
5V
R225
TP205
C218
MAIN DEEMPH
PRE AMP
C209
FL201
L.P.F
R213
R214
SUB L.P.F
DEM
DOUBLE LIM
DOC ENV DET
PB FM
(350mVp-p)
C224
R239
PB EQ
C239-241
L207-208
R240
FROM H/A BLOC
PB FM
* 4 4HEAD MODELS
7 2HEAD MODELS
C225
C216
C215
L201
C214
R224
R226
R229
5V
R201
PB LEV ADJ
D202
"L" CARRIER INTERLEAVE OFF
NLY 2HEAD LONG PLAY MODELS & 4HEAD MODELS
CC
AX
18
SP (H)
18
Q204
SP-SW
FROM
SYSTEM CTL

PB LUMINANCE SIGNAL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES



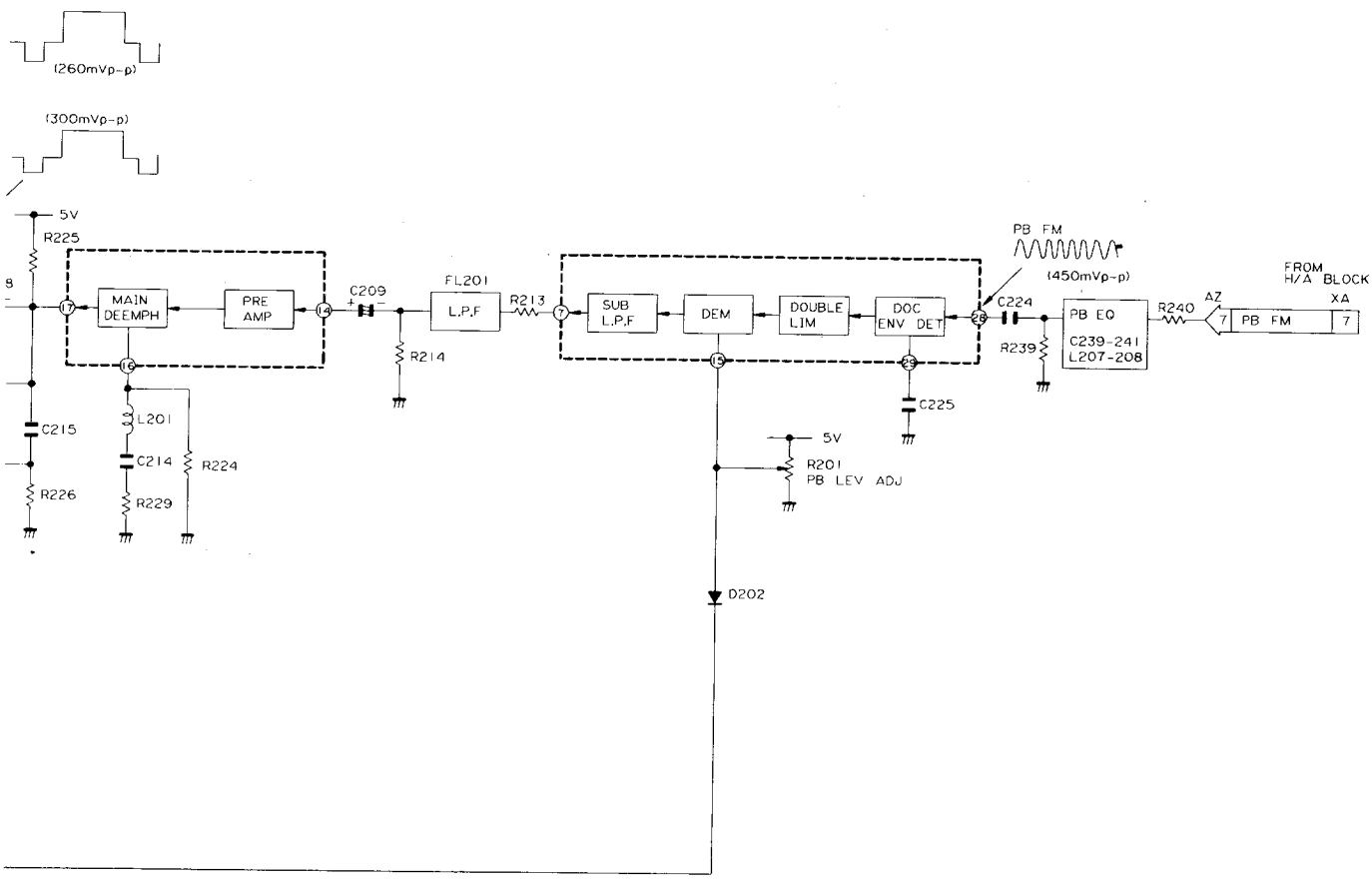

551
AMP
E.F
Q5552
Q5553
Q5554
H/A SW
1H DL
Q5555
FV SW
CA
AV
1
H/A SW
1
FROM
SYSTEM CTL
CA
AV
3
FV CTL
3
FROM
SYSTEM CTL
CC
AX
16
LP (H)
16
FROM
SYSTEM CTL
ONLY 4-HEAD
MODELS
BURST 300mVp-p
8532
C531
FL502
4.43MHz
B. P. F
R525
R533
R531
SW
CARR
BAL
MAIN
CONV
ACC
AMP
ACC
DET
D502
(PB mode established in IC
by AL 5V applied at pin 16)
C523
L503
L504
Q507
AMP
CE
XA
PB CHROMA
* 5 2HEAD MODELS
6 4HEAD MODELS
R541
C536
C537
C538
L. P. F
C524
C513
C516
BURST 150mVp-p
ONLY MODELS FOR D.E.N
Q5502
SECAM MUTE
CB
AW
8
MESECAM (H)
8
FROM
SYSTEM CONTROL
BLOCK
FL501
5.06MHz
B.P.F
C515
90°
ROTATTION
SUB
CONV.
NTSC
SECAM
PAL SW
H NTSC
M SECAM
L PAL
CB
AW
9
CHROMA ROT.
9
FROM
SYSTEM CTL
Q509
APC SW
R515
CB
AW
14
AL PB 5V
14
FROM
SYSTEM CTL
ONLY MESECAM (ONLY MODELS WITH MESECAM RECORDING & PLAYBACK)
IC5001 (BA7007)
SECAM
(H)
PC 9V
R5503
ID
SIG.
GATE
LIM.
1/2th
AMP
R5510
C5503
R5509
D5503
R5506
D5502
C5504
R5507
R5508
PC 9V
Q5501
INV.
FL5501
C5506
L5502
C5507

PB CHROMINANCE SIGNAL BLOCK DIAGRAM
VC-A30/A35/A40/A45 SERIES
VC-A50/A60/A61/A62 SERIES

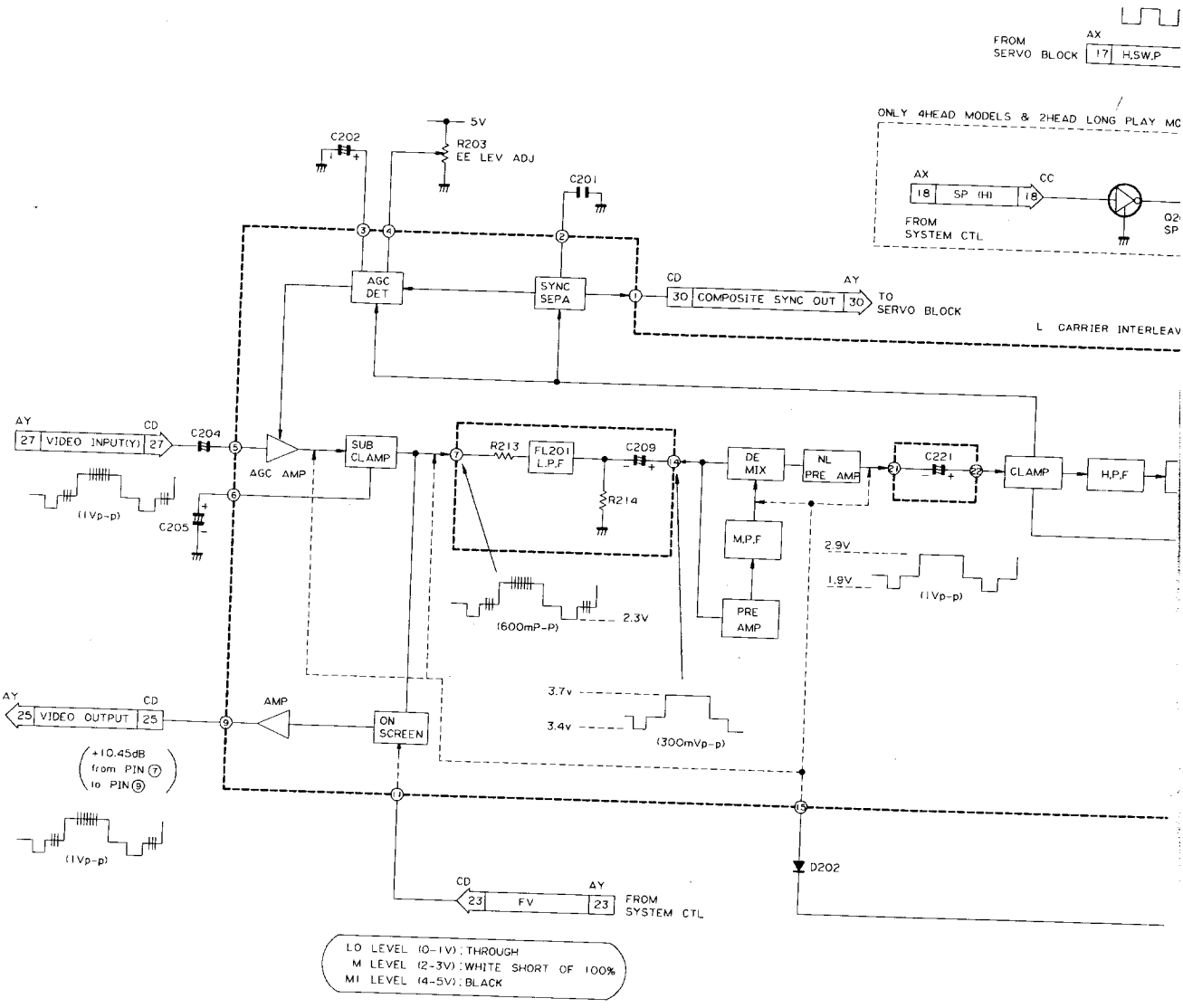


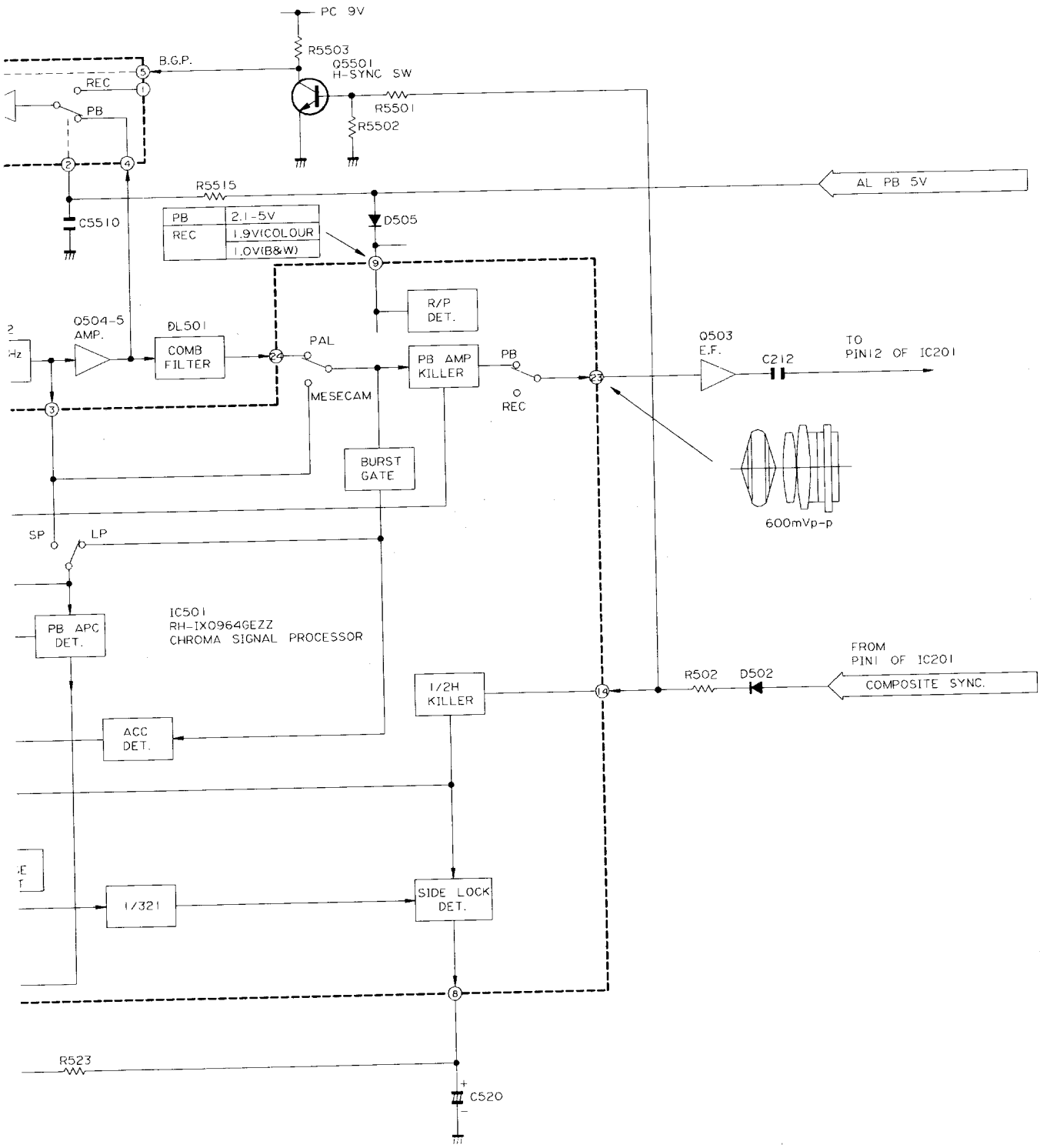
Note ALL tereminal signal levels typical values.

* CCD Charge Coupled Device

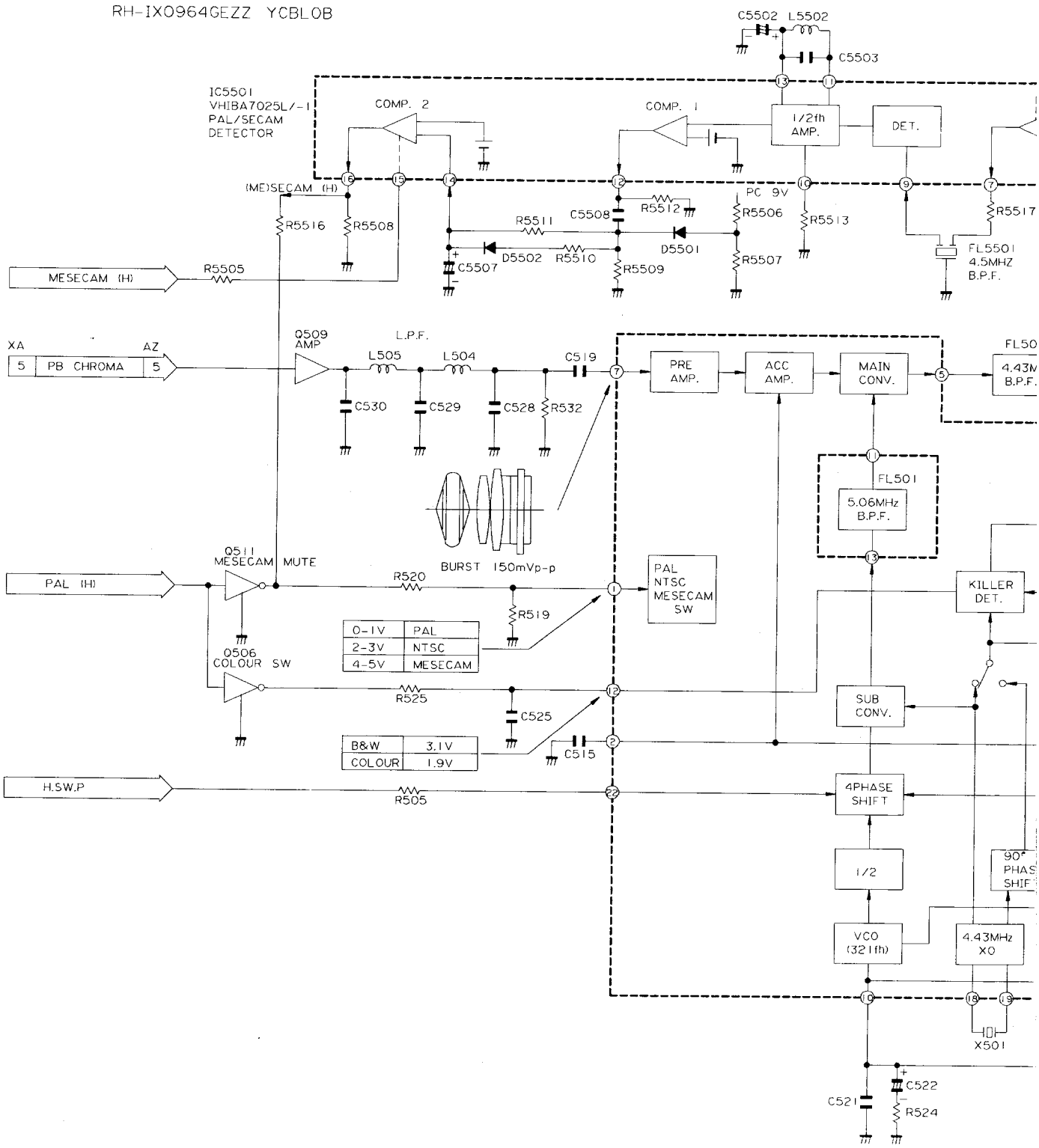


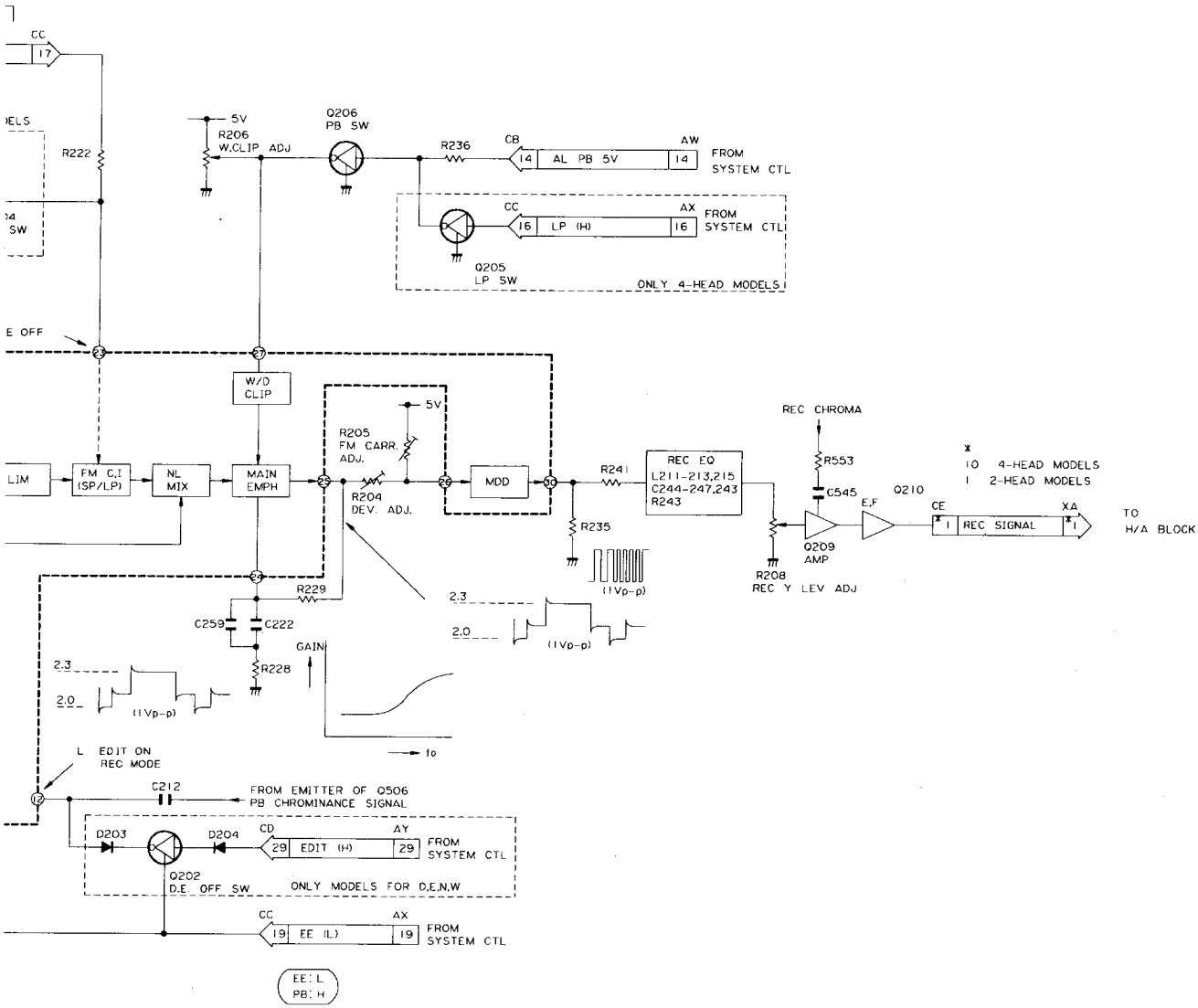
REC LUMINANCE SIGNAL BLOCK DIAGRAM
VC-A30/A35/A40/A45 SERIES
VC-A50/A60/A61/A62 SERIES



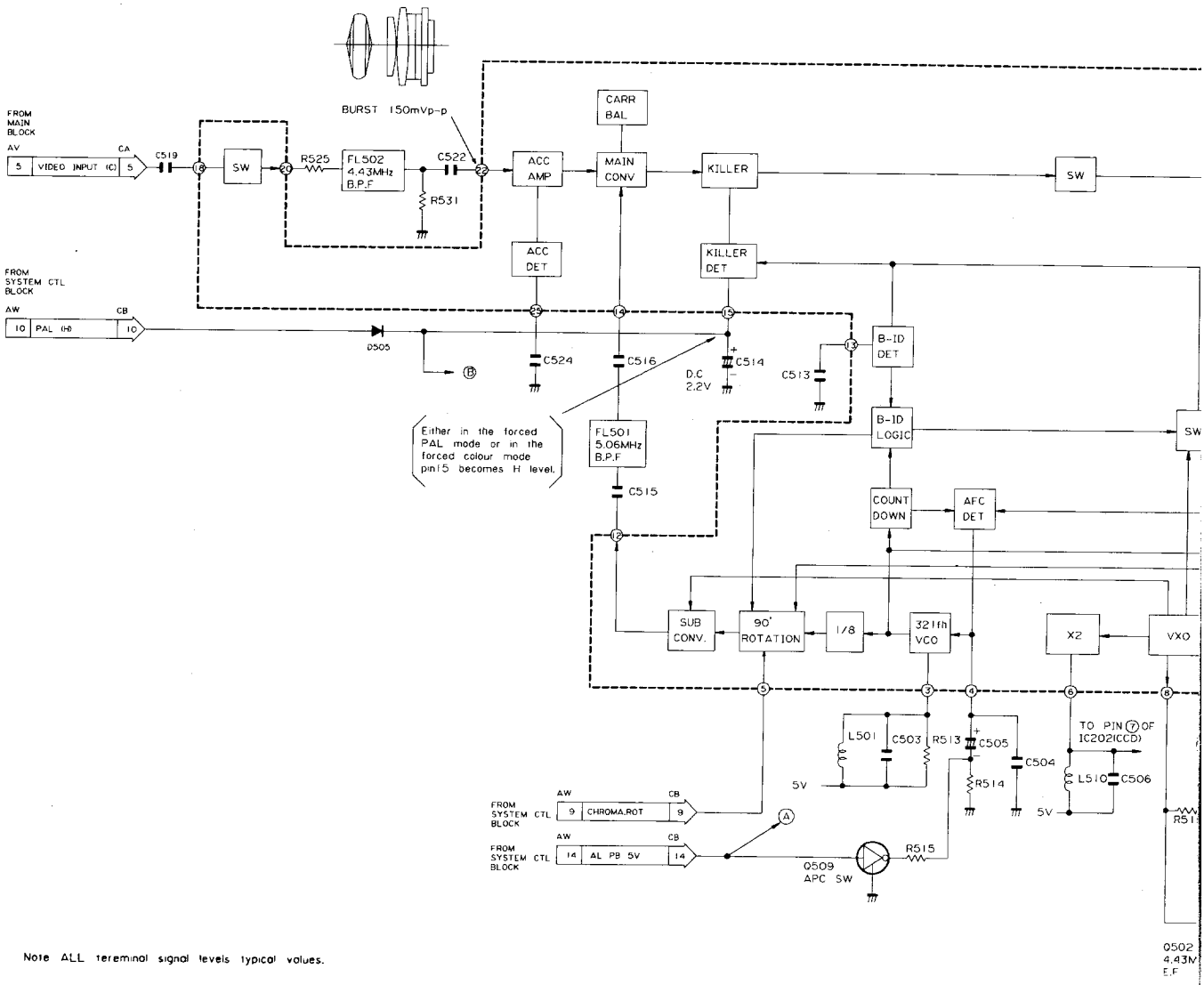

PC 9V
R5503
Q5501
H-SYNC SW
R5501
R5502
B.G.P.
REC
PB
R5515
AL PB 5V
C5510
PB 2.1-5V
REC 1.9V(COLOUR
1.0V(B&W)
D505
R/P DET.
Q504-5 AMP.
DL501
COMB FILTER
PAL
MESECAM
PB AMP KILLER
PB
REC
Q503 E.F.
C212
TO PIN12 OF IC201
600mVp-p
BURST GATE
SP
LP
IC501
RH-IX0964GEZZ
CHROMA SIGNAL PROCESSOR
PB APC DET.
ACC DET.
1/2H KILLER
R502
D502
FROM PIN1 OF IC201
COMPOSITE SYNC.
1/321
SIDE LOCK DET.
R523
C520

PB CHROMINANCE SIGNAL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES

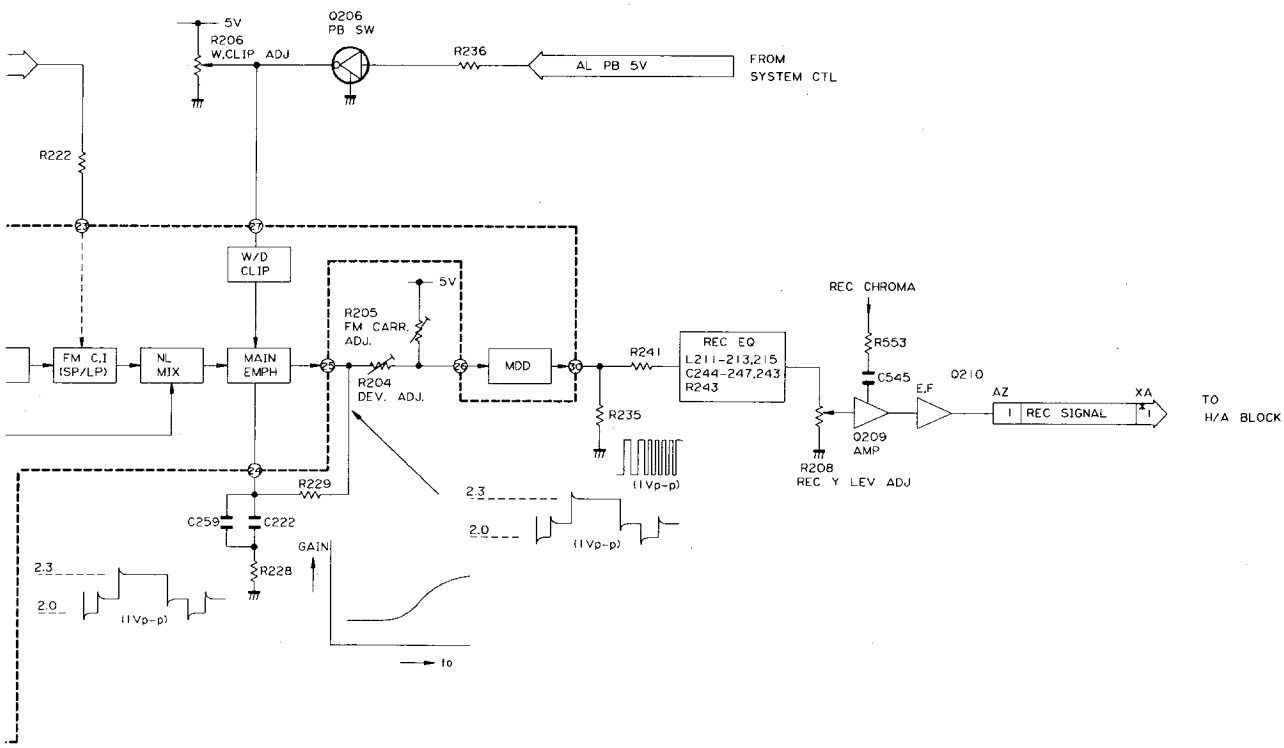



CC
17
R222
5V
R206
W.CLIP ADJ
Q206
PB SW
R236
CB
14
AL PB 5V
14
AW
FROM
SYSTEM CTL
CC
16
LP (H)
16
AX
FROM
SYSTEM CTL
Q205
LP SW
ONLY 4-HEAD MODELS
E OFF
W/D
CLIP
5V
R205
FM CARR.
ADJ.
R204
DEV. ADJ.
MDD
R241
REC EQ
L211-213,215
C244-247,243
R243
REC CHROMA
R553
C545
Q210
E,F
CE
1
REC SIGNAL
1
XA
TO
H/A BLOCK
10 4-HEAD MODELS
1 2-HEAD MODELS
Q209
AMP
R208
REC Y LEV ADJ
R235
(1Vp-p)
R229
C259
C222
R228
GAIN
2.3
2.0
(1Vp-p)
fo
L EDIT ON
REC MODE
C212
FROM EMITTER OF Q506
PB CHROMINANCE SIGNAL
D203
D204
CD
29
EDIT (H)
29
AY
FROM
SYSTEM CTL
Q202
D.E. OFF SW
ONLY MODELS FOR D,E,N,W
CC
19
EE (L)
19
AX
FROM
SYSTEM CTL
EE: L
PB: H

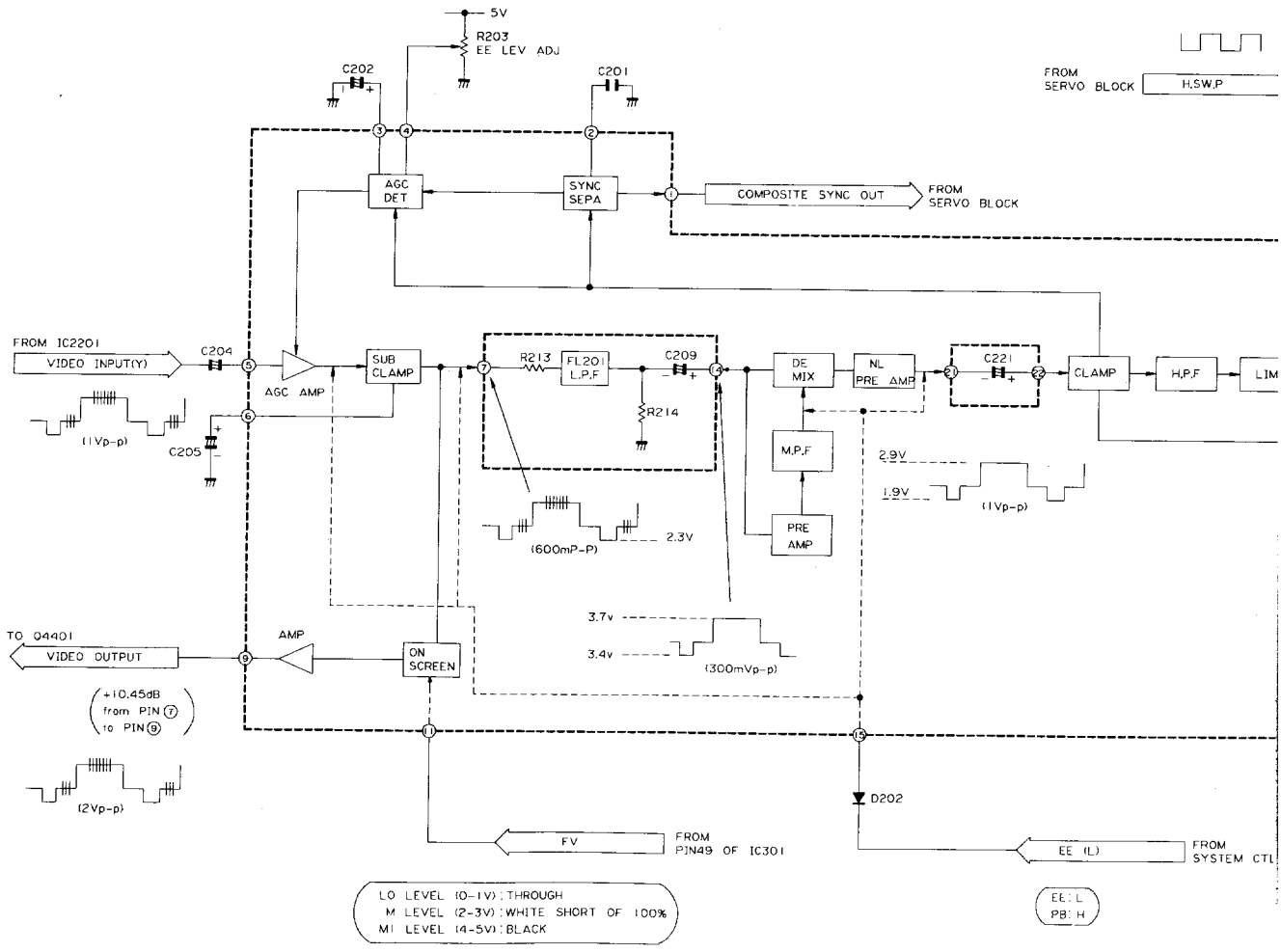
REC CHROMINANCE SIGNAL BLOCK DIAGRAM
VC-A30/A35/A40/A45 SERIES
VC-A50/A60/A61/A62 SERIES

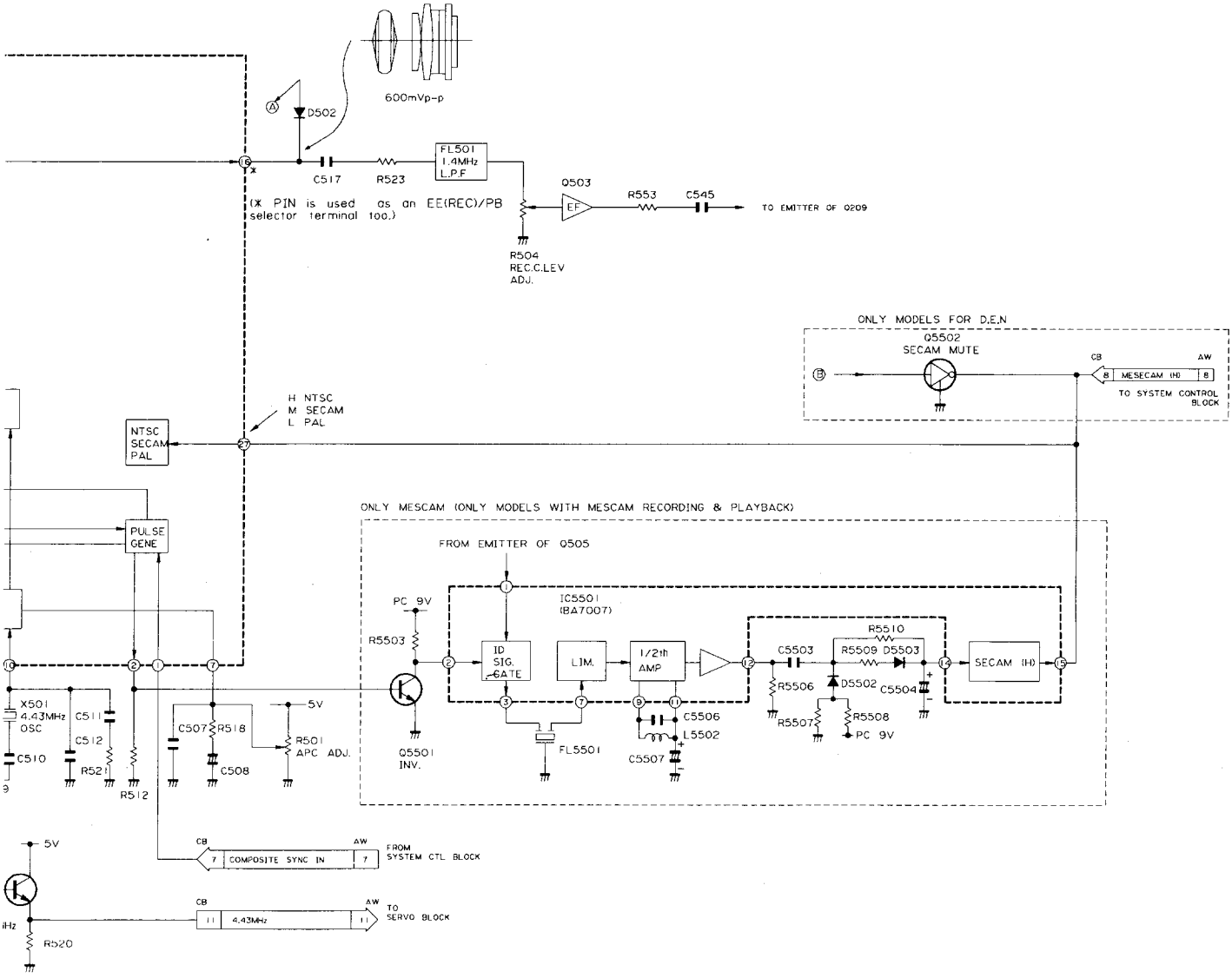


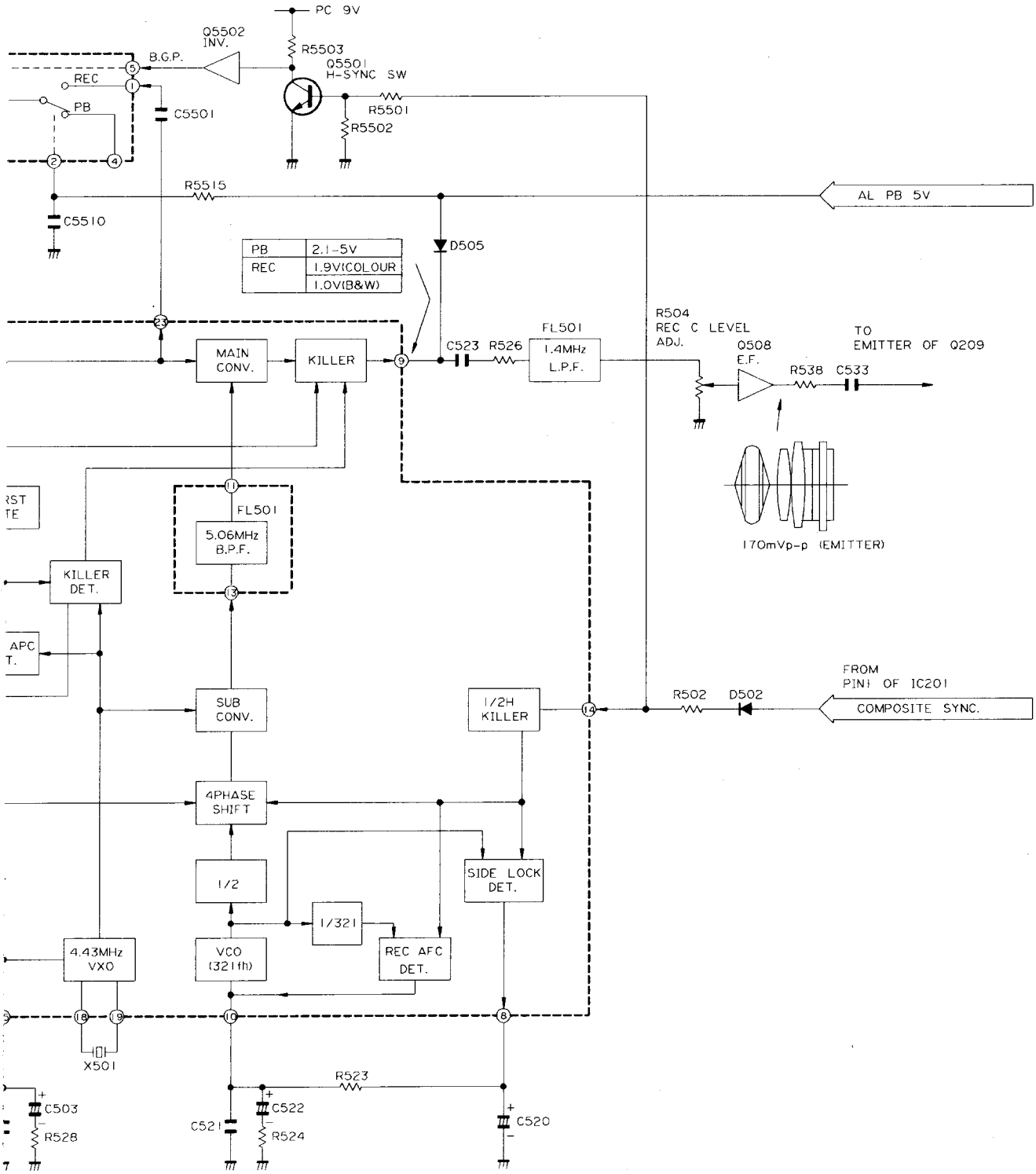
Note ALL tereminal signal levels typical values.


5V
R206
W.CLIP ADJ
Q206
PB SW
R236
AL PB 5V
FROM
SYSTEM CTL
R222
W/D
CLIP
5V
R205
FM CARR.
ADJ.
FM C.I
(SP/LP)
NL
MIX
MAIN
EMPH
R204
DEV. ADJ.
MDD
R241
REC EQ
L211-213,215
C244-247,243
R243
REC CHROMA
R553
C545
Q210
E.F
AZ
XA
REC SIGNAL
TO
H/A BLOCK
R235
(1Vp-p)
Q209
AMP
R208
REC Y LEV ADJ
R229
C259
C222
R228
GAIN
2.3
2.0
(1Vp-p)
2.3
2.0
(1Vp-p)
to

REC LUMINANCE SIGNAL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES




600mVp-p
D502
FL501
1.4MHz
L.P.F
C517
R523
(* PIN is used as an EE(REC)/PB selector terminal too.)
Q503
EF
R553
C545
TO EMITTER OF Q209
R504
REC.C.LEV
ADJ.
ONLY MODELS FOR D,E,N
Q5502
SECAM MUTE
CB
AW
MESECAM (H)
TO SYSTEM CONTROL BLOCK
H NTSC
M SECAM
L PAL
NTSC
SECAM
PAL
PULSE
GENE
ONLY MESCAM (ONLY MODELS WITH MESCAM RECORDING & PLAYBACK)
FROM EMITTER OF Q505
PC 9V
R5503
IC5501
(BA7007)
ID
SIG.
GATE
LIM.
1/2th
AMP
C5503
R5510
R5509 D5503
SECAM (H)
R5506
D5502
C5504
R5507
R5508
PC 9V
C5506
L5502
C5507
FL5501
Q5501
INV.
X501
4.43MHz
OSC
C511
C512
R521
C510
R512
C507
R518
C508
5V
R501
APC ADJ.
5V
CB
AW
7
COMPOSITE SYNC IN
FROM
SYSTEM CTL BLOCK
11
4.43MHz
TO
SERVO BLOCK
R520


PC 9V
Q5502
INV.
B.G.P.
R5503
Q5501
H-SYNC SW
REC
PB
C5501
R5501
R5502
R5515
AL PB 5V
C5510
D505
PB 2.1-5V
REC 1.9V(COLOUR
1.0V(B&W)
R504
REC C LEVEL
ADJ.
FL501
1.4MHz
L.P.F.
C523 R526
MAIN
CONV.
KILLER
Q508
E.F.
TO
EMITTER OF Q209
R538 C533
170mVp-p (EMITTER)
FL501
5.06MHz
B.P.F.
KILLER
DET.
APC
T.
SUB
CONV.
1/2H
KILLER
R502 D502
FROM
PIN1 OF IC201
COMPOSITE SYNC.
4PHASE
SHIFT
1/2
1/321
SIDE LOCK
DET.
4.43MHz
VXO
VCO
(321fh)
REC AFC
DET.
X501
R523
C503
R528
C521
C522
R524
C520

REC CHROMINANCE SIGNAL BLOCK DIAGRAM (FOR 2-HEAD MODELS) : VC-A10 SERIES